CHAPTER 27

DETECTION AND AUTOMATIC VOLUME CONTROL

By B. Sandel, A.S.T.C.

SECTION 1 : A-M DETECTORS

(i) Diodes (A) General (B) Diode curves (C) Quantitative design data (D) Miscellaneous data (ii) Other forms of detectors (A) Grid detection (B) Power grid detection (C) Plate detection (D) Reflex detection (E) Regenerative detectors (F) Superregenerative detectors.

(i) Diodes

(A) General

A diode has two electrodes namely plate and cathode. It is therefore identical in structure with a power rectifier but the term is generally restricted to valves which are used for detection or a.v.c. as distinct from rectifiers which are used for power supply. The operation of diodes with a.v.c. is considered in detail in Sect. 3 of this chapter. The operation of a diode on a modulated wave is rather different from the operation of a power rectifier, and it is necessary to consider the characteristic curves of a diode valve if a full understanding of the operation is to be obtained. The operation of diodes on a modulated input is considered in (B) below. Fig. 27.1 shows typical distortion curves for a diode operating firstly under ideal conditions with no a.c. shunting (curve B) and secondly the distortion resulting when a load of 1 megohm is shunted across a diode load resistance of 0.5 megohm (curve A). The respective percentages of harmonic distortion at 100% modulation are approximately 6% and 12% so that the presence of such shunting has a very marked effect on performance ; these curves apply only for the particular conditions under which they were derived.

The design of a diode detector for low distortion is based on the following requirements :

(1) That the input voltage should not be less than 10 volts peak.

(2) That no appreciable a.c. shunting should be present.

The first of these two requirements is easily met for local stations and a voltage from 10 to 20 volts is quite common in receivers fitted with a.v.c. The second requirement is one which is difficult to satisfy. Shunting of the diode load may be due to :

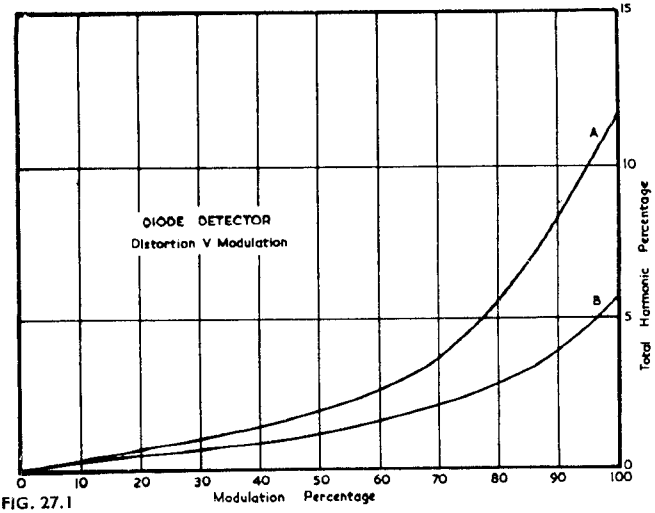


FIG. 27.1

(1) The a.v.c. system.

(2) The following grid resistor.

(3) An electron ray tuning indicator.

The circuit of a typical diode detector is shown in Fig. 27.2 in which the diode load resistance is R_2 together with R_1 ; the latter, in conjunction with C_1 and C_2, form a r-f filter so that the r-f voltage passed on to the a-f system may be a minimum. R_1 is generally made about 10% of R_2 and typical values are 50 000 ohms and 0.5 megohm. The capacitances of C_1 and C_2 depend upon the frequency of the carrier ; for an intermediate frequency of 455 Kc/s they may both be 100 $\mu\mu$F.

If the volume control (R_2) is turned to maximum the shunting effect due to R_3 will be appreciable, since R_3 cannot exceed 1 or 2 megohms with most types of valves. If, however, grid leak bias is used on a high-mu triode valve, R_3 may be approximately 10 megohms and the input resistance of the valve will then be of the order of 5 megohms. This is sufficiently high to be unimportant but for lower values of R_3 the distortion with the control set near maximum may be severe. It is found in most conventional receivers that the a-f gain is considerably higher than that required for strong carrier voltages and under these conditions the control will be turned to a low setting. The a.c. shunting effect due to R_3 is practically negligible provided the control is below one-fifth of the maximum position. A good method of overcoming the a.c. shunting due to the audio amplifier is shown in Fig. 27.3. The diode may be in the same envelope as the i-f amplifier valve. Negative feedback is applied across part of the cathode bias resistor for the a-f voltage amplifier valve. For the component values shown, the measured input resistance between points A and B is in excess of 10 megohms for frequencies up to about 10 Kc/s. A possible disadvantage is the reduction in overall gain because of the negative feedback, although this is not generally serious. Increasing the feedback resistance R increases the overall gain, but reduces the input resistance. Intermediate values of gain and input resistance may be selected as desired. For further details of receivers using this arrangement see Refs. 6 and 7.

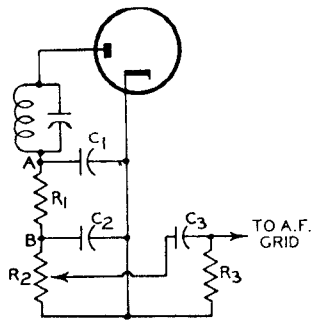


FIG. 27·2 DIODE DETECTOR CIRCUIT

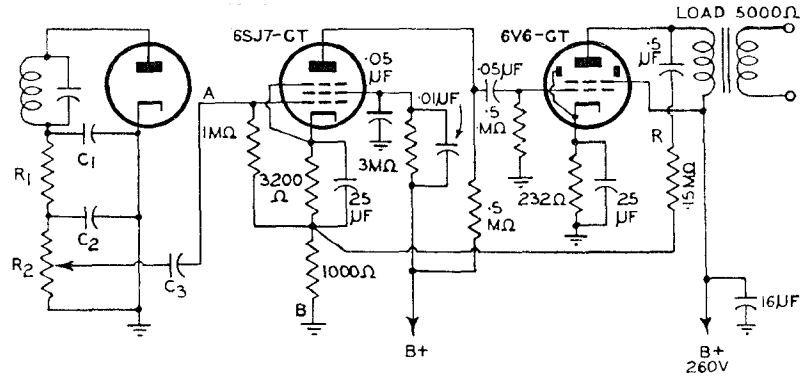


FIG. 27·3 AUDIO AMPLIFIER GIVING LOW A.C. SHUNTING ACROSS DIODE LOAD.

Another useful method of reducing a.c. shunting effects is to use a cathode follower stage between the detector and the a-f voltage amplifier. This is often conveniently accomplished by employing a double triode valve, one section serving as the cathode follower and the other as an a-f voltage amplifier.

Distortion due to the a.v.c. system will be discussed in detail in Sect. 3 below. One type of distortion often encountered is caused by delayed a.v.c. systems at the point where the a.v.c. diode just starts to conduct. This form of distortion is called differential distortion and may be kept to low values by making the delay voltage small. The conventional arrangement for obtaining a.v.c. voltage from the primary of the last i-f transformer is generally preferred, as it reduces the a.c. shunting effect across the detector diode circuit.

The a.c. shunting due to the addition of an electron ray tuning indicator to the diode detector circuit is serious and difficult to avoid. In order to reduce the distortion to a minimum the resistor feeding the grid of the tuning indicator may be made 2 megohms and the effect will only then be apparent at high percentages of modulation. If the tuning indicator is connected to the a.v.c. system it will not operate at low carrier levels unless the delay voltage is extremely small. One possible method, where the utmost fidelity is required, is to use the same circuit as for delayed a.v.c. but with a delay voltage of zero, and to connect the tuning indicator to this a.v.c. circuit. With this arrangement a.c shunting due to the a.v.c. circuit and the tuning indicator is eliminated, while differential loading no longer occurs.

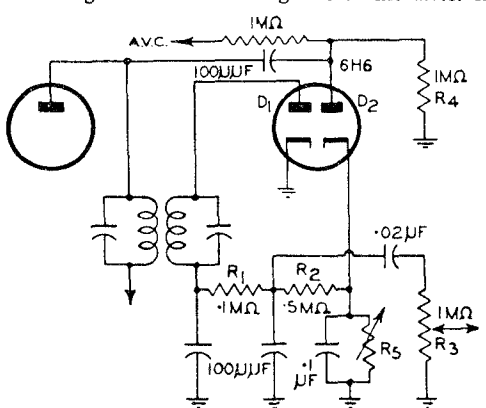


FIG. 27·4 COMPENSATED DIODE DETECTOR.

An interesting arrangement (Ref. 8) for counteracting the effect of a.c. loading, and so increasing the maximum percentage of modulation which can be handled without excessive distortion is accomplished by the use of the circuit of Fig. 27.4. In this arrangement a positive bias is applied to the diode plate in such a way as to be proportional to the carrier input. A fixed positive bias would not be satisfactory since it would only give low distortion at one carrier level.

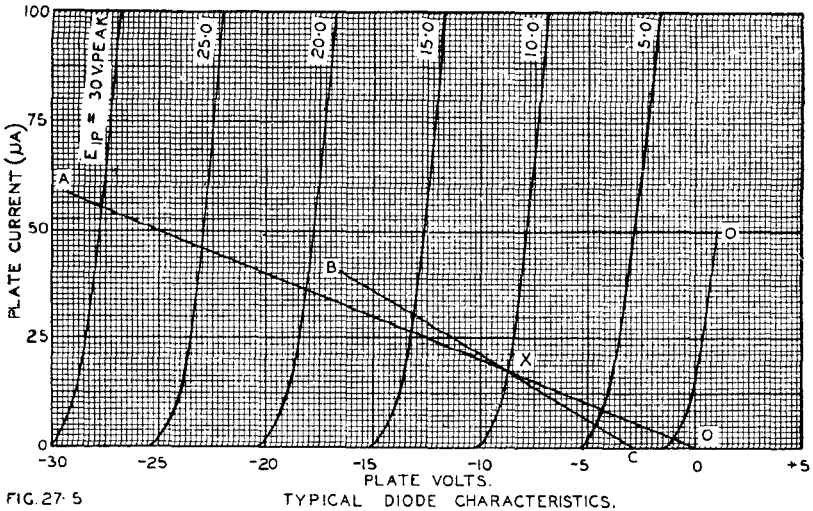


FIG. 27·5 TYPICAL DIODE CHARACTERISTICS.

(B) Diode curves

Typical diode characteristics are shown in Fig. 27.5. Each curve corresponds to the peak voltage of a constant unmodulated carrier voltage. On this graph may be drawn loadlines corresponding to diode load resistances in a similar manner as for triodes. The intersection of the applied loadline (OA) with the peak input voltage curve indicates the d.c. voltage developed by the diode and available for a.v.c. As the load resistance increases, so the d.c. voltage approaches the peak input voltage.

For example, if the carrier input is 10 volts peak and the diode load resistor 0.5 megohm, the diode current will be 17 μA, and the d.c. voltage —8.7 volts. If 100% modulation is applied to the carrier, the operating point will move at audio frequency along the loadline from the intersection with the "0" curve, through X to the intersection with the 20 volt curve. The distortion over this excursion is small (about 5% second harmonic) and may be reduced still further by operating with a higher carrier input voltage.

Typical diode curves with loadlines already drawn are shown in valve data books. Average curves are shown in Fig. 27.6 and these are applicable to the diodes incorporated in standard types of Radiotron diode-triode and diode-pentode valves. It has become the usual practice to show the signal input voltages in r.m.s. values rather than the peak voltages indicated in Fig. 27.5.

If the d.c. load resistance of 0.5 megohm, represented by *OA* in Fig. 27.5, is shunted by an a.c. load (such as would occur due to the grid resistor of the following valve) the dynamic loadline will be similar to *BC*, which passes through the static point *X* but which has a slope corresponding to the total effective a.c. load resistance. This loadline (*BC*) reaches cut-off at about 75% modulation and the distortion at higher percentages of modulation will consequently be severe. For any combination of d.c. and a.c. loads it is possible to draw the loadlines and determine the limiting percentage of modulation before distortion becomes excessive. It should not be overlooked that there will be some distortion present even before the limiting percentage of modulation is reached. The evaluation of this distortion is discussed below.

(C) Quantitative design data

Design formulae will be set out below so that the performance of the diode detector circuit can be assessed. These expressions are used in conjunction with the diode curves of Fig. 27.6. The design procedures are necessarily a series of compromises but the results form a useful practical guide. For a more detailed discussion the reader is referred particularly to Ref. 1 (p. 339), Ref. 2 (p. 413) and Ref. 5 (p. 553).

(a) **Diode detection efficiency**

This can be found from curves such as those shown in Fig. 27.6. The efficiency (assuming a sine wave input) is

$$\eta = \frac{E_{dc}}{\sqrt{2}E_{rms}}. \tag{1}$$

Suppose the d.c. load is 0.5 megohm and the signal input (E_{rms}) is 15 volts (r.m.s.). Then from the curves $E_{dc} = 16.8$ volts.

$$\eta = \frac{16.8}{\sqrt{2} \times 15} = 0.793 \text{ or } 79.3\%.$$

Actually the a.c. load should be determined and used for all calculations. The a.c. load is, from Fig. 27.2,

$$R_{ac} = R_1 + \frac{R_2R_3}{R_2 + R_3} \tag{2}$$

The d.c. load for the diode detector is

$$R_{dc} = R_1 + R_2. \tag{3}$$

If simple a.v.c. is used the effect of additional a.c. shunting due to this circuit should be taken into account. In this case the effects of additional capacitive reactance are usually neglected for simplicity.

(b) **Critical modulation ratio**

The highest percentage of modulation which can be handled by the detector, before serious distortion of the modulation envelope occurs, is given by

$$m = 1 - \eta F \frac{R_{dc}}{R_{dc} + R_3/F} \tag{4}$$

where F = fraction of R_{dc} across which R_3 is tapped

$$= \frac{R_2}{R_1 + R_2} = \frac{R_2}{R_{dc}}.$$

If $R_{dc} = 0.5$ MΩ, made up from $R_1 = 50\,000$ Ω and $R_2 = 0.45$ MΩ, then $F = 0.45/0.5 = 0.9$. Taking $\eta = 0.793$ as before, and $R_3 = 1$ MΩ we have,

$$m = 1 - 0.793 \times 0.9 \frac{0.5}{0.5 + 1/0.9} = 0.78 \text{ or } 78\%.$$

It should be noted that the smaller F is made, the higher the critical modulation ratio. If F is fixed, then R_3 is made as large as possible but is usually limited to about 1 or 2 megohms unless special circuit arrangements, such as those discussed previously, are made.

The critical modulation ratio can also be increased by applying a positive d.c.

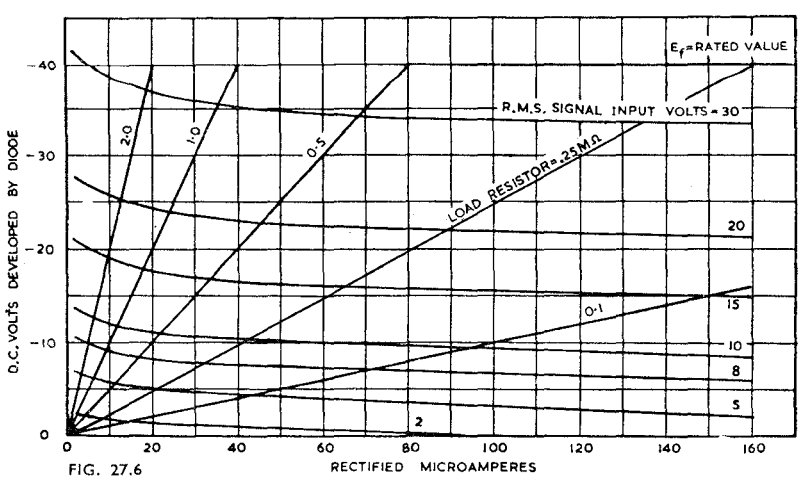


FIG. 27.6

bias voltage to the diode plate. This arrangement is only satisfactory if the bias can be changed for each i-f input voltage (E_{rms}) see Ref. 1 (page 348).

For this case

$$m = \left(\frac{\sqrt{2}E_{rms} + E_{bias}}{\sqrt{2}E_{rms}}\right)\left(1 - \eta F\frac{R_{dc}}{R_{dc} + R_3/F}\right) \quad (5)$$

The circuit of Fig. 27.4 shows a practical arrangement for increasing the critical modulation ratio by applying positive bias to the diode plate, as mentioned previously in Sect. (A) above.

(c) **Equivalent damping across i-f transformer**

The secondary circuit damping is found approximately from

$$R_E = \frac{R_{ac}(\sqrt{1 - \eta^2} - \eta \cos^{-1}\eta)}{\eta(\cos^{-1}\eta - \eta\sqrt{1 - \eta^2})}. \quad (6)$$

R_E/R_{ac} can be read directly from Fig. 27.7 for various values of η.

Suppose $R_{ac} = 0.36$ MΩ and $\eta = 0.793$ then, since $R_E/R_{ac} = 0.7$, the equivalent damping resistance is $R_E = 0.7 \times 0.36 = 0.25$ MΩ.

It is often taken in practice (as a " rule of thumb ") that the equivalent damping resistance is half the d.c. diode load resistance. This gives an equivalent damping resistance of $R_{dc}/2 = 0.5/2 = 0.25$ MΩ in this case. However, it should be realized that if the diode efficiency is taken as unity, the equivalent damping resistance which appears across the tuned circuit is half the a.c. load resistance ; this is indicated by Fig. 27.7.

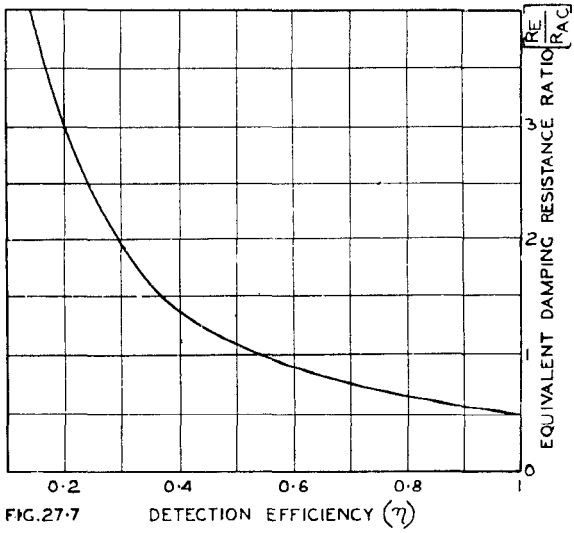


FIG.27·7

Damping of the i-f transformer primary is serious when the a.v.c. voltage is derived from a diode detector connected to this voltage source. The usual arrangement is a capacitor (100 $\mu\mu$F or less) taken from the plate connection of the transformer primary to the diode plate. The additional primary damping from this source is approximately one third of the d.c. load resistance for the a.v.c. diode. This also follows fairly readily if it is considered that R_{dc} shunts the primary of the transformer, and in addition the diode conduction current also adds damping equivalent to a parallel resistance of approximately $R_{dc}/2$. From this

$$R_E = \frac{R_{dc}(R_{dc}/2)}{R_{dc} + R_{dc}/2} = \frac{R_{dc}}{3}.$$

For a typical case, the a.v.c. resistance would be 1 megohm, and so the equivalent damping resistance would be approximately 0.33 megohm. If the i-f amplifier valve

has a plate resistance of 0.8 megohm the primary damping resistance would be 0.23 megohm.

This means that, with detector and a.v.c. diodes conducting, both the secondary and primary circuits of the i-f transformer are heavily damped and this damping must be taken into account when the i-f transformer, connected between the last i-f voltage amplifier valve and the diode detector, is being designed. Delayed a.v.c. will, of course, affect the primary circuit damping and three conditions arise : the diode not conducting, the diode just starting to conduct, and the diode conducting when the applied voltage is reasonably large. When conduction just starts the damping depends very largely on the diode detection efficiency and will vary quite appreciably for a small range of input voltages. It is usually sufficient, however, to know the tuned circuit damping for the two conditions, diode not conducting, and diode conducting with a reasonably large input voltage. For the diode not conducting the added damping is approximately R_{ac} ; R_{dc} should not be used here. With the diode conducting the added damping can be taken as $R_{dc}/3$ with sufficient accuracy in some cases since in this case the fact that the diode detection efficiency is not unity offsets to some extent the increase in damping which is obtained when R_{ac} is used in place of R_{dc}.

Damping of the transformer tuned circuits as determined above assumes linear diode plate-voltage—plate-current characteristics. For parabolic diode detection the damping differs by only a small amount from that given by the linear characteristics and so, in practice, it is seldom necessary to treat the two cases separately. In any case the order of accuracy to be expected in the final results from the procedures set out, would hardly justify any additional refinements in the design calculations.

(d) **The actual degree of modulation**

The degree of modulation applied to the detector is always less than the modulation of the incoming carrier. The actual value of m which the detector will be required to handle is given approximately by

$$m = m' \frac{R_3(R_{dc} + 2Z_L)}{R_{dc}R_3 + 2Z_L(R_{dc} + R_3)} \qquad (7)$$

where m' = original modulation percentage

R_{dc} = $R_1 + R_2$ (see Fig. 27.2)

R_3 = grid resistor of following stage (see Fig. 27.2)

and Z_L = load impedance presented to the i-f voltage amplifier preceding the detector stage ; including the effects of all damping on the primary and secondary of the i-f transformer.

In addition, at higher audio frequencies the reduction of side band amplitude by the selectivity of the earlier stages in the receiver results in a further decrease in depth of modulation.

(e) **Audio frequency output voltage and response** (frequency distortion)

The approximate r.m.s. audio frequency output voltage can be determined for a particular arrangement by using the equivalent circuit of Fig. 27.8. It is often assumed that all capacitive reactances are negligible, for simplicity in carrying out gain calculations. However, the circuit is readily modified to include C_1, C_2 and C_3 as

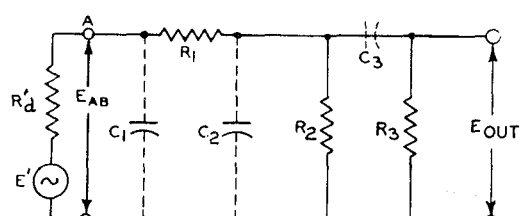


FIG. 27·8 EQUIVALENT DIODE CIRCUIT AT AUDIO FREQUENCIES.

shown by the dotted lines, and any additional capacitances in the circuit can be included if necessary. For this diagram

m = modulation factor
E_{rms} = i-f input voltage
η = detection efficiency determined from curves of Fig. 27.6
Z = total load impedance connected between the terminals AB. (This is equal to R_{ac} over the middle audio frequency range)

$$R_{ac} = R_1 + \frac{R_2R_3}{R_2 + R_3}$$

and R'_d = internal equivalent resistance of diode at audio frequencies. This is given by the inverse slope of the curves of Fig. 27.6.

R_1, R_2 and R_3 are as shown in Fig. 27.2.

It should be noted that R'_d is not the diode conduction resistance (R_d) but is related to it by

$$R'_d = \frac{\pi R_d}{\cos^{-1}\eta}. \tag{8}$$

Also R'_d and R_d are not constant for all operating conditions. For our previous example we see from the 15 volt (r.m.s.) curve of Fig. 27.6, and taking the diode load as being

$$R_1 + R_2 = 0.5 \text{ M}\Omega, \text{ for simplicity,}$$

$$R'_d = \frac{(17 - 16.5) \times 10^6}{(42 - 26)} = 31\,200\ \Omega.$$

It will be seen that R'_d is determined in a rather similar manner to that used for finding the plate resistance of multi-element valves. The diode conduction resistance in this case is (approximately) 6500 ohms.

It is sometimes required to find the audio frequency response and this can readily be determined from the complete circuit of Fig. 27.8. A suitable procedure would be as for r.c. amplifiers in which the capacitances are ignored over the middle frequency range (say around 400 to 3000 c/s), and the audio voltage output is calculated for the resistance network only. At low frequencies the effects of C_1 and C_2 can be ignored since they are usually about 50 to 100 $\mu\mu$F each, and only the effect of C_3 would be considered. At high frequencies C_3 would be neglected and the effects of C_1 and C_2 considered. Often only the maximum output voltage is required plus the total output variation from say 50 c/s to 10 Kc/s, and this simplifies the calculations. If Fig. 27.8 is inspected it will be seen that it is a simple matter to apply the generalized low frequency response curves given in Chapter 12. The high frequency curves can also be applied directly if R_1 can be neglected (this is usually permissible) and C_1 and C_2 are considered as being in parallel.

When using the circuit of Fig. 27.8 it is more convenient to determine the voltage E_{AB} since this is given directly by

$$E_{AB} = \eta m E_{rms}.$$

It follows that, over the middle frequency range,

$$E_{out} = E_{AB}\left(\frac{R_{ac} - R_1}{R_{ac}}\right)$$

and $$\frac{E_{out}}{E'} = \frac{E_{out}}{E_{AB}} \times \frac{E_{AB}}{E'} = \frac{R_{ac} - R_1}{R_{ac} + R_d}.$$

If R_1 can be neglected in comparison with R_2 and R_3 in parallel, then $E_{out} = E_{AB}$ over the middle frequency range.

It is more accurate to determine E_{AB} from the curves of Fig. 27.6, since η is not constant for a modulated carrier voltage and the effects of contact potential are included in the measured data. The procedure is to draw the a.c. loadline on the graph and note the d.c. voltages E_{dc_1} and E_{dc_2} given by the maximum and minimum values of E_{rms} during modulation. From this

$$E_{AB} = \frac{1}{2\sqrt{2}}(E_{dc_1} - E_{dc_2}).$$

The simplified graphical procedure is only suitable when the amplitudes of harmonics higher than the second are negligible [see also (h) below]. More accurate graphical methods are required if this is not true.

To compare the results obtained by the two methods, assume $E_{rms} = 15$ volts and the percentage modulation is 50% (i.e. $m = 0.5$). As determined previously $\eta = 0.793$, and it will be taken that $R_{ac} = R_{dc} = 0.5$ megohm. Then

$$E_{AB} = \eta m E_{rms} = 0.793 \times 0.5 \times 15 = 5.95 \text{ volts (r.m.s.).}$$

From Fig. 27.6, $E_{dc1} = 26.5$ volts and $E_{dc2} = 7.5$ volts so that

$$E_{AB} = \frac{1}{2\sqrt{2}} (26.5 - 7.5) = 6.7 \text{ volts.}$$

The discrepancy between these two results is easily explained, as an examination of typical diode circuits giving the d.c. voltage developed by the diode in the absence of signal input shows that there is about -0.5 to -1 volt developed across a diode load of 0.5 megohm. This difference is also illustrated by the curve of Fig. 27.5, which shows that -1 volt is developed for the conditions being considered. It is also seen that the variation in detection efficiency (η) over the range of voltage used does not have a large effect on the final result. The presence of d.c. voltage across the load resistor, in the absence of signal input voltage, is due to contact potential in the diode.

(f) **Effect of shunt capacitance on detection efficiency**

Too low a value for C_1 and C_2 will affect the detection efficiency. Provided the **total** shunt capacitance across the diode load is not less than $\frac{12.72}{fR_{ac}}$ $\mu\mu$F the effect can be neglected where

f = frequency (expressed in Mc/s)

$$R_{ac} = R_1 + \frac{R_2 R_3}{R_2 + R_3} \text{ (expressed in M}\Omega\text{).}$$

For our previous example of $R_{ac} = 0.36$ MΩ, and i-f of 455 Kc/s, the capacitance due to C_1 and C_2 should not be less than about 78 $\mu\mu$F ; this includes all stray capacitances. In the circuit of Fig. 27.2 typical values of C_1 and C_2 are 100 $\mu\mu$F each and if R_1 is neglected it is seen that the total capacitance is more than twice the value required even when strays are neglected. It would be feasible to reduce C_1 and C_2 to 50 $\mu\mu$F respectively with a reduction in attenuation at the higher audio frequencies.

(g) **Non-linear distortion**

If the value of total capacitance across the diode load resistance is too large, the discharge time constant will be too long and the voltage across the diode load will not follow the modulation envelope. This will give rise to non-linear distortion and suggests that the rate of discharge of the load circuit should not be less than the maximum rate of change of the modulation envelope. It can be shown that non-linear a-f distortion due to this cause can be almost completely avoided provided that

$$\frac{1}{\omega C_t R_{dc}} \gg m. \tag{9}$$

Suppose we neglect the decoupling resistance (R_1) in Fig. 27.2, as this unnecessarily complicates calculations when its value is about 1/10 of R_2 (the usual case).

What is required, is to determine a value for $C_t R_{dc}$ which will allow $m = 1$, i.e. the incoming signal to be 100% modulated. However, it should be clear from previous discussion that the modulation percentage is generally a good deal lower than this figure, and it seldom happens that very high modulation percentages occur at high audio frequencies.

Take R_{dc} as 0.5 megohm, then $1/\omega C_t = mR_{dc} = 1 \times 0.5 \times 10^6$.

Assume that the highest audio frequency is 10 Kc/s, then $\omega = 2\pi \times 10^4$ and so

$$C_t = \frac{10^{12}}{2\pi \times 10^2 \times 0.5 \times 10^2} = 31.8 \ \mu\mu\text{F.}$$

This is the largest value C_t should have if the detector is to be capable of handling audio frequencies of 10 Kc/s and 100% amplitude modulation.

It will be noticed from (e) above that the detector efficiency will be reduced if C_t is

given the value determined. A suitable practical compromise would be to make $C_1 = C_2 = 50\ \mu\mu F$ and retain the values of R_1, R_2 and R_3 given in the example. If improved decoupling is required then R_L could be increased to say 0.1 megohm This also permits a higher critical modulation ratio at the expense of some reduction in available audio output. The difficulty with non-linear distortion is not encountered when C_t is charging, since the diode is conducting and the charging time constant is approximately $C_t R'_d$ which in our example is, taking $C_t = 100\ \mu\mu F$, $100 \times 10^{-12} \times 3.12 \times 10^4 = 3\,12\ \mu$ secs. The discharge time constant is approximately $100 \times 10^{-12} \times 0.5 \times 10^6 = 50\ \mu$ secs.

(h) **Estimate of magnitude of non-linear distortion**

The distortion can be found from the curves of Fig. 27.6 in the same way as for power amplifiers (Ref. 3, p. 100). The operating point corresponding to a given signal input is marked on the a.c. loadline. The maximum and minimum excursions of the modulation envelope are now marked on this same line. If only second harmonic distortion is required (and higher order harmonic distortion is very small) these points are sufficient. For distortion calculations which involve harmonics higher than the second the methods detailed in Chapter 13 should be used. The expression to be used here is

$$\text{2nd harmonic percentage} = \frac{1}{2}\left(\frac{A-1}{A+1}\right) \times 100\%, \qquad (10)$$

$$\text{where } A = \frac{\text{positive current swing}}{\text{negative current swing}}.$$

Voltage swing would give the same results, since the load is taken as being a pure resistance.

Suppose we take $R_{ac} = R_{dc}$ and use the 0.5 MΩ loadline. The carrier input voltage is 15 volts (r.m.s.) and is modulated 50%. The voltage swing is thus $\pm$ 7.5 volts (r.m.s.) about 15 volts.

From Fig. 27.6 this gives (approximately)

$$A = \frac{53 - 33.5}{33.5 - 16} = 1.11$$

$$\text{2nd harmonic percentage} = \frac{1}{2}\left(\frac{0.11}{2.11}\right) \times 100 = 2.6.$$

The true a.c. loadline would indicate somewhat more distortion than is given by this simple example.

(D) Miscellaneous data

(a) With radio receivers using diode-triode or diode-pentode valves as combined detectors and a-f or i-f amplifiers several effects require consideration. Where the combined valve is used in the a-f application, difficulty is often experienced with **residual volume effect** (" play-through "). This effect is quite distinct from the minimum volume effect experienced with receivers using a reflexed amplifier. The residual volume is heard in the receiver output when the audio volume control is turned to zero (the grid may also be earthed as a further check). The cause of the effect is capacitive and electronic coupling between the detector diode and the plate of the a-f voltage amplifier.

In some cases there may be direct coupling at audio frequencies, but usually the important factor is coupling of modulated i-f currents which are detected in the audio amplifier.

A complete cure for the trouble is to combine the detector diode with the i-f voltage amplifier. However, this can sometimes lead to difficulties with regeneration or degeneration at i-f due to coupling between the detector diode and signal grid. When the valve is retained as an a-f amplifier it is necessary to keep all stray coupling to a minimum by careful layout and wiring. Diode pentodes are often helpful, particularly when series screen feed is used, as adequate screen by-passing gives a marked improvement. Adequate cathode circuit by-passing is essential in all cases. Neutralization to reduce the effect is almost useless unless rather elaborate circuits are used. In some cases different types of sockets offer an improvement. If simple a.v.c. is used,

earthing, or even leaving disconnected, the second diode will often effect an almost complete cure. Obviously the diode connection nearest the plate of the voltage amplifier is the one which should be earthed.

A second effect which is less frequently encountered is residual volume due to capacitance between a diode and the control grid of a combined detector and a-f amplifier. Normally this capacitance is unimportant because with the volume control turned right down the control grid is grounded through the grid coupling capacitor (see Fig. 27.2). However if the audio amplifier is grid leak biased it may have a 10 megohm grid leak, and in this case a 0.001 μF grid coupling capacitor would give adequate bass response for a small receiver. Under these conditions a voltage of the order of one thousandth of the i-f input to the diode could appear on the control grid and with a high gain receiver this is ample to give annoying minimum volume. The remedy, of course, is to increase the size of the grid coupling capacitor.

(b) In general, diodes do not start to conduct at precisely the point where the plate voltage exceeds zero. **Contact potentials** and other effects will sometimes allow the valve to conduct when the diode plate voltage is slightly negative (this is usual with valves having indirectly heated cathodes), but in other cases (e.g. some battery valves) conduction does not occur until the plate voltage is appreciably positive. This point can be appreciated by an examination of typical diode curves. The effects of the contact potentials will be further considered in Sect. (3) below when automatic volume control is being discussed.

For a discussion of the effects of positive and negative start of plate current (which may be deliberately introduced as mentioned in (C)(b) above) in diode detectors the reader is referred to Ref. 1, Chapter 8.

(c) There are distinct advantages in having the **a-f volume control as the diode load**. For the usual operating conditions on local signals the setting of the control is fairly well down, and so the effects of a.c. loading are very much reduced. This advantage is lost when the control is in the grid circuit of the a-f voltage amplifier. The disadvantage is that many controls become noisy, usually after a fairly short period, when they have the diode current passing through them. A compromise arrangement may be best with the control in the grid circuit (R_3 in Fig. 27.2) and R_1 about 0.1 megohm and R_2 say 0.5 megohm.

(d) As a summary of the characteristics of the diode detector, it may be stated that its performance as regards frequency and non-linear distortion is excellent provided the input voltage is high and the factors discussed above regarding a.c. shunting etc. are incorporated in the detector design. All forms of detectors suffer from distortion at low input levels, but the diode has the particular advantage that the input may be increased to a very high level with consequent reduction of distortion, without any overloading effect such as occurs with other forms of detectors.

(e) **Crystal diodes** are described in Section 7.

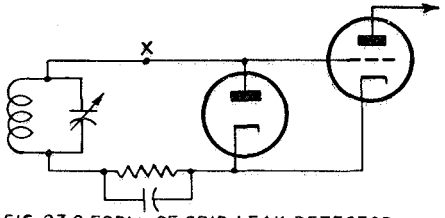


FIG. 27.9 FORM OF GRID LEAK DETECTOR.

(ii) Other forms of detectors

(A) Grid detection

Leaky grid or " cumulative detection " has been used for many years and is still widely used for certain applications. The theory of its operation is essentially the same as that of the diode except that a triode is also used for amplification. The derivation of a leaky grid detector from the combination of a diode and triode is shown in Fig. 27.9. Whether the grid capacitor and resistor are inserted as

shown (as is usual with the diode) or at the point X is immaterial from the viewpoint of operation. The diode is directly coupled to the triode and therefore the audio frequency voltages developed in the diode detector are passed on to the triode grid, but at the same time this grid is given a d.c. bias through the d.c. voltage developed in a similar way to that by which a.v.c. is obtained. Consequently the operating point of the triode varies along the e_g-i_p curve from zero towards more negative grid bias voltages as the carrier voltage is increased. This is the same effect as that obtained when the diode is omitted (Fig. 27.10) since the grid and cathode of the triode act as a diode and produce the same results. The illustration given was purely to demonstrate the derivation of the one from the other and not to be a practical form of detector since no advantage is gained by retaining the diode in the circuit.

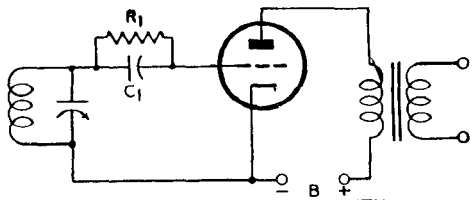


FIG.27·10 GRID LEAK DETECTOR WITH TRANSFORMER COUPLING.

It will be seen that the operating point varies along the e_g-i_p characteristic curve between zero bias and the cut-off point (Fig. 27.11). There will be a certain strength of carrier at which the detection will be most satisfactory, and at lower or higher levels detection will not be so satisfactory on account of improper operating conditions. If with a certain carrier input voltage the d.c. bias on the grid is OA, then the point corresponding to peak modulation is B where OB equals twice OA. If the point B is on the curved part of the characteristic, or in the extreme case actually beyond the cut-off, the distortion will be severe. A valve having low μ and low g_m is capable of operating with a higher carrier voltage than a valve with improved characteristics, but the gain in the detector stage will be less. There is a further difficulty in that the plate current at no signal, or at very weak signal, may be excessively high. If transformer coupling is used this may, in extreme cases, damage the valve, or pass too much direct-current through the transformer, unless the plate supply voltage is reduced. If resistance coupling or parallel-feed is used the efficiency of the detector is decreased. As with diode detection there is distortion at low levels due to the "diode characteristics" but as distinct from the diode, the overload point occurs at quite a low carrier voltage. This method of detection is therefore very much limited in application.

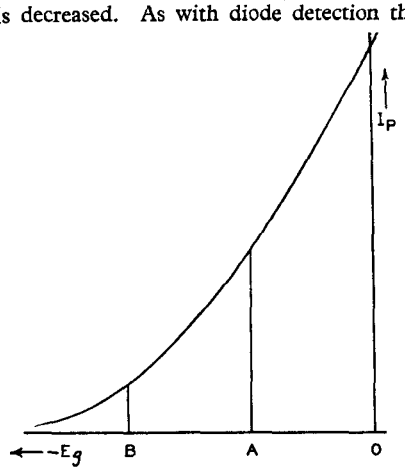


FIG.27·11 TYPICAL E_g-I_p CHARACTERISTIC.

With battery type valves used as cumulative grid detectors it is often advantageous to connect R_1 (Fig. 27.10) to filament positive; C_1 remains as before. The advantage obtained is that larger modulation percentages can be handled and detection will start with smaller input voltages. The arrangement is equivalent to supplying the grid, which is acting as the plate of a diode, with a positive bias voltage (see Ref. 1, p. 357) and moving the position of the start of grid current.

A typical circuit for a grid leak detector as used in radio receivers is shown in Fig. 27.12.

Damping of the input circuit occurs in the same manner as for a diode but additional damping occurs because of grid-plate coupling. The arrangement shown in Fig. 27.12 for the grid resistor further increases the loading on the input circuit. Detailed discussions of this type of circuit can be found in Refs. 2 (p. 414), 1 (p. 377) and 10.

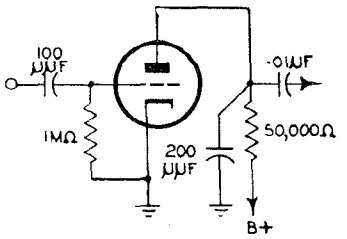


FIG. 27·12· TYPICAL GRID LEAK DETECTOR WITH R-C COUPLING.

(B) Power grid detection

Power grid detection is a modification of leaky grid or cumulative detection and the circuit is identical in form, but the operating conditions are so chosen that the valve will operate on higher carrier voltages without overloading. In order to obtain a short time constant from the grid capacitor and resistor combination the capacitance and resistance are reduced, thereby improving the high audio frequency response. Under optimum conditions the distortion is at least as high as that of a diode together with increased distortion due to the curvature of the e_g-i_p characteristic. The overload point, even though higher than that of ordinary leaky grid detection is at a much lower level than that with diode detection.

All forms of grid detection, particularly " power grid detection," involve damping of the grid circuit due to grid current, and this damping causes loss of sensitivity and selectivity. Grid detection is thus similar to diode detection in that it damps the input circuit. It has the advantage over diode detection in that gain is obtained in the detector which can be still further increased if transformer coupling is used between it and the following stage. Transformer coupling can, of course, only be used when the valve has a low plate resistance.

The foregoing comparison between a diode and a grid detector is on the basis of the detector alone. In modern practice the diode detector is frequently in the same envelope with a voltage amplifier and the total gain is quite high.

(C) Plate detection

Plate detection or " anode bend detection " involves operation towards the point of plate current cut-off so that non-linearity occurs, thereby giving rectification. Owing to the slow rate of curvature the detection efficiency is small, but there is an advantage in that the amplification which is obtained makes up, to a certain extent, for the poor detection efficiency. Due to the gradual curvature the distortion is very great with low input voltages, and even with the maximum input before overload occurs the distortion is rather high with high percentages of modulation. An important advantage of plate detection is, however, that the grid input circuit is not damped to any great extent, and the detector is therefore sometimes spoken of as being of infinite impedance, although this term is not strictly correct.

With pentode valves it is possible to use either " Bottom Bend Rectification " as with triodes or " Top Bend Rectification " peculiar to pentodes. This " top bend " in resistance coupled pentode characteristics can be seen on valve data sheets e.g. type 6J7 dynamic $e_g - i_p$ characteristics provide a good illustration (Fig. 12.14A).

A similar effect occurs with triodes, but only in the positive grid region, and for this reason it is incapable of being used for plate rectification. For top bend rectification with a pentode valve it is desirable to operate the valve with a plate current in the region

of 0.95 (E_B/R_L). The exact operating point for optimum conditions depends upon the input voltage.

Pentode valves are particularly valuable as plate detectors since the gain is of such a high order. If resistance coupling is used the gain is reduced very considerably, and in order to eliminate this loss it is usual to adopt choke coupling using a very high inductance choke in the plate circuit, shunted by a resistor to give a more uniform frequency response. If the shunt resistor were omitted the high frequencies would be much greater than the low frequencies in relative level.

With all forms of plate detectors the bias is critical and since different valves of the same type require slightly different values of bias the use of fixed bias is not recommended. A very high value of cathode resistance is usually adopted to bias the valve very nearly to cut-off, and in such a way that if valves are changed, or vary during life, the operating point maintains itself near optimum (Fig. 27.13).

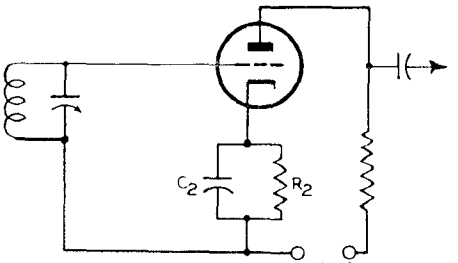


FIG. 27·13 PLATE DETECTOR.

Screen grid and pentode valves with self-bias have been used as plate detectors very satisfactorily for a number of years, although the distortion with the usual arrangement is too high for them to be used in any but the cheapest radio receivers at the present time. Such a detector is, however, permissible for some types of short-wave reception and for amateur communication work where its high grid input impedance results in higher sensitivity and selectivity.

With the usual plate detector the cathode bypass capacitor (C_2, Fig. 27.13) has customarily been made sufficiently large to by-pass both audio and radio frequencies. Often C_2 is a 25 μF electrolytic in parallel with a 500 $\mu\mu$F mica capacitor. This arrangement, although widely used in the past, is not a correct one and leads to distortion when the modulation factor is at all high. The effect is similar to that described in connection with diode detectors having the a.c. loadline appreciably different in slope from the d.c. loadline. The correct procedure calls for the resistor R_2 to be by-passed for radio frequencies only, and although this results in a very considerable loss in gain because of negative feedback, the results obtainable are excellent. In a typical case R_2 might be taken as 10 000 to 100 000 ohms and C_2 as 500 to 100 $\mu\mu$F respectively, the plate load resistor would be about 0.25 megohm ; additional r-f decoupling is usual in the plate circuit, although this is not shown in Fig. 27.13. This circuit is often called a reflex detector, although this term is sometimes reserved for cases where 100% negative feedback is used with a plate detector, and the audio output is then taken from the resistor in the cathode circuit ; the plate is earthed for a.c. in this case. The results obtainable from the modified plate detector are excellent, and are comparable with those given by the diode arrangement. The reflex detector is further discussed below.

(D) Reflex detector

The reflex detector is essentially a plate detector with negative feedback. Any amount of feedback may be applied from zero to 100%, and as the feedback increases, so the distortion decreases and the stage gain decreases until in the final condition with 100% feedback the gain is less than unity. The reflex detector has an even higher input impedance than the usual type of plate detector, and is therefore valuable in certain applications. Under certain conditions the input resistance is negative and can lead to instability troubles. The increased selectivity can also result in side-

band cutting. The degree of feedback may be adjusted to give any required gain (within reasonable limits) by altering the size of cathode by-pass capacitor and the relationship between the plate and cathode load resistance, but the distortion increases with gain and if low distortion is required the maximum gain is limited to about three or four times even with a pentode valve. With maximum degeneration and stable operating conditions, the distortion (see Ref. 11) is about the same as for a diode operating under similar input voltage conditions, while the reflex detector has the distinct advantage of high input impedance. One application which appears to be of importance is in high fidelity t.r.f. receivers, but even here the reflex detector has not shown any very marked improvement over the diode from a consideration of distortion alone. Input voltages in the order of 10 volts (r.m.s.) are usually most satisfactory when low distortion is desired and in a typical case using 100% feedback about 3% total harmonic distortion can be expected when the modulation depth approaches 100%. This assumes that the a.c. shunting is high (say 10 : 1 or so) compared with the d.c. load. Some useful discussion is given in Refs. 14 (pages 51-55) and 15. These performance figures can be compared with those stated previously for the diode detector under similar operating conditions. Reflex detectors do not provide a.v.c. and so are not used in normal broadcast receivers. They could be used in combination with amplified a.v.c. to provide a receiver with good characteristics.

Typical circuit component values have been discussed in (C) above in connection with modified plate detectors. For the case of 100% negative feedback (i.e. the load resistance is in the cathode circuit and the plate is earthed for a.c.) the cathode resistance is made large compared with $1/g_m$ and a typical value is 25 000 ohms. The by-pass capacitance across this resistance can be about 500 $\mu\mu$F. There is seldom any difficulty with a.c /d.c. ratios as the grid resistance of the following a-f stage is generally about 0.5 megohm. Additional components required are a blocking capacitor, to prevent the d.c. cathode voltage from being applied to the grid of the a-f amplifier, and a series resistor and shunt capacitor to provide additional r-f decoupling between the two circuits.

A limitation of the reflex detector is that there is a definite maximum for the input signal voltage for freedom from grid current. A further increase of input causes rectification at the grid, with added damping of the grid input circuit, and a steady increase in distortion. An increase in the supply voltage raises the threshold point for grid current. Further data are available in Refs. 11, 12, 13, 14 and 15.

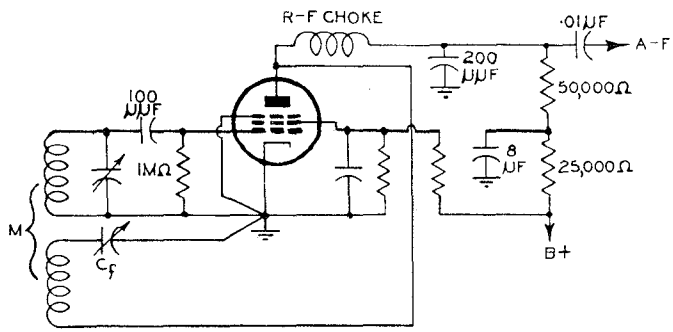


FIG. 27·14 REGENERATIVE DETECTOR.

(E) Regenerative detectors

A common arrangement for this type of detector is shown in Fig. 27.14. The amount of positive feedback is adjustable, by means of C_f, to allow increased sensitivity with various signal input voltages. Oscillation will occur when the degree of feedback is sufficiently large, and the circuit can then be used for the detection of CW telegraph signals. For battery operated valves it is usual to return the grid resistor to filament positive.

Best results are generally obtained using pentode valves and resistance-capacitance coupling to the following audio stage. This arrangement minimizes " threshold howl."

Feedback control is possible with a variety of circuits but least difficulty is usually experienced with the variable capacitor arrangement, or the use of a variable resistor in the screen circuit. The latter arrangement is advantageous as regards the reduction of detuning effects.

Further details of this type of detector can be found in Refs. 1, 5, 16, 17, 18, 19 and 20.

(F) Superregenerative detectors

The superregenerative detector is a regenerative circuit in which the detector is automatically switched in and out of oscillation at a very low radio frequency rate (usually about 15 to 100 Kc/s). This switching frequency is called the " quenching " frequency. In general the quenching frequency is increased as the carrier frequency becomes greater, but sensitivity and selectivity are improved by using the lowest permissible value of quenching frequency. For many cases it is usual to make the quench frequency about twice the highest audio frequency contained in the modulation envelope, and it is not considered good practice for the quench frequency to be lower than this value. The amplitude of the quench voltage is also important and it will have a very appreciable effect on the selectivity characteristic. In general if the quench voltage amplitude is increased in a separately quenched circuit, the selectivity is reduced.

The advantage of this circuit is the extremely high sensitivity which is possible using a single valve. The disadvantages are the high noise level in the absence of a signal, the poor selectivity, and the high distortion.

The circuit of Fig. 27.14 can be made to operate as a superregenerative detector by increasing the time constant of the grid resistance and capacitance combination, and making the amount of regeneration very large. The quenching frequency can be simply adjusted by altering the value of the grid resistance.

A separate quenching oscillator is often used with the regenerative detector arrangement, but as this requires additional circuit components and sometimes an additional valve, it is not so popular as the simple arrangement previously mentioned. The development of suitable types of double triode and converter valves largely overcomes this objection, however, and many modern circuits use separate quenching.

Several other points of interest arise with this detector. Amplitude limiting occurs, so there is less interference from car ignition and similar noises than when other detectors are used ; the output on strong signals is not much greater than for weak signals. Noise quieting and limiting are improved however, by using low quench frequencies. A r-f stage should be incorporated in receivers using this type of detector to reduce radiation. This additional stage will not materially alter the signal-to-noise ratio obtainable with the detector alone. Circuits incorporating the principle of superregeneration have been used in cheap F-M receivers ; this point will receive some further consideration in the section on F-M receivers in Chapter 36.

The method to be adopted for measuring the selectivity of a superregenerative receiver requires some consideration. Conventional methods are usually inadequate since in most cases the problem is similar to that of taking the selectivity curve of a receiver having a.v.c., but in this case the a.v.c. cannot be disconnected. A suitable procedure (Ref. 26) is as follows.

With no input signal applied the audio noise output is measured. A signal is applied at the resonance frequency and its amplitude adjusted until the noise is suppressed by about 10 to 20 db (or any convenient amount). The selectivity is then found by tuning the signal generator to various frequencies around resonance, in the usual manner, and the input voltage is adjusted until the same degree of quieting is obtained as at resonance. The difference between the two signal inputs off and at resonance for the same degree of quieting, gives the attenuation at the particular frequency being considered.

Further details of this detection system are available in page 622 of Ref. 5, page 148 of Ref. 20, Refs. 21, 22, 23, 24, 25, and 26.

SECTION 2 : F-M DETECTORS

(i) Types of detectors in general use (ii) General principles (iii) Phase discriminators (A) General (B) Design data (C) Design example (iv) Ratio detectors (A) General (B) Operation (C) Types of circuit (D) Design considerations (E) Practical circuits (F) Measurements on ratio detectors.

(i) Types of detectors in general use

Although many ingenious methods have been suggested for the detection of frequency modulated signals, only a few circuits have found general acceptance by receiver manufacturers. Of these detectors a form of locked oscillator (the Bradley detector) has been used by one large manufacturer, but does not appear to have been employed to any extent outside of this organization. Amplitude discriminators have been used to a very limited extent with duo-diode triode valves having a separate cathode for the two diodes. However, the generally accepted method of F-M detection has been **the phase discriminator**. A modification of the basic phase discriminator circuit has been used for **the ratio detector,** and this arrangement has achieved wide popularity because it allows a satisfactory F-M receiver to be constructed without the use of an additional amplitude limiting stage. Simple detuning of the signal circuits has been employed in one type of receiver (the **Fremodyne**) to give frequency to amplitude conversion, but this is only satisfactory in a very cheap receiver where cost is more important than quality.

In what follows attention will be confined, mainly, to the design procedures to be adopted for phase discriminators and ratio detectors. References are listed at the end of this chapter, and can be consulted for details of a number of the alternative detection systems available. The amplitude and phase discriminators used in connection with Automatic Frequency Control Systems are further considered in Chapter 29.

(ii) General principles

The circuits which will be considered here utilize tuned circuits to convert frequency changes to amplitude changes. The amplitude modulated carrier is then applied to detectors (usually diodes) to recover the intelligence contained in the received signals.

Although the amplitude modulated carrier applied to the detectors is also frequency modulated, the detectors are only sensitive to amplitude changes, and so it is only the resultant amplitude variations which appear at the output of the detector stage. It is because the detectors are sensitive to amplitude changes, that some method of limiting is required to overcome undesired amplitude variations.

The tuned circuits to be described are called discriminators, although this name is often taken to include the diode detectors as well. If distortion is not to be introduced by the discriminator it is essential that the amplitude variations produced be directly proportional to the frequency variations i.e. the circuit must be linear over the full range of applied frequency deviation. The usual precautions for reducing distortion in the detector circuits must also be applied, just as for any other A-M detector. These precautions have been discussed previously, and those given for diode detectors should be carefully observed here. One big advantage does appear, however, the percentage amplitude modulation is likely to be quite small, depending on the frequency-amplitude conversion efficiency of the discriminator circuit, and so the possibility of non-linear distortion is considerably reduced.

(iii) Phase discriminators

(A) General

The basic circuit arrangement, together with the voltage distribution at the resonant frequency, for a phase discriminator is shown in Fig. 27.15. The name arises because the operation is dependent on the 90° phase shift which occurs at resonance between the primary and secondary voltages of a tuned transformer. When the frequency of the applied primary voltage $\mathbf{E}_1$ (the magnitude of this voltage will be

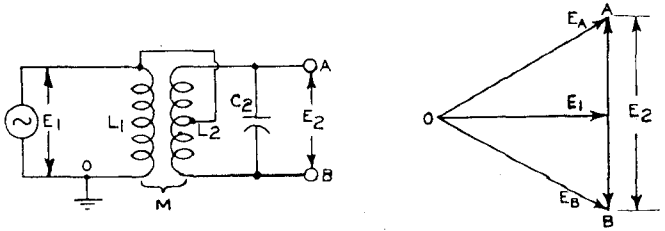


FIG. 27·15 BASIC PHASE DISCRIMINATOR CIRCUIT.

assumed constant for the moment) alters, the phase angle between $\mathbf{E}_1$ and $\mathbf{E}_2$ changes from that at resonance. This leads to a change in the relative magnitudes of $\mathbf{E}_A$ and $\mathbf{E}_B$.

The vector relationship between the primary and half secondary voltages, for the phase discriminator, are shown in Fig. 27.16. This assumes constant primary voltage $\mathbf{E}_1$.

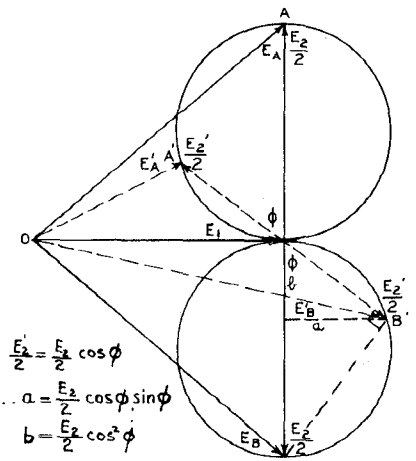


FIG. 27·16 VOLTAGE RELATIONSHIPS IN PHASE DISCRIMINATOR WITH CONSTANT PRIMARY VOLTAGE.

If the primary voltage $\mathbf{E}_1$ has its amplitude varied in a suitable manner (e.g. by setting the coupling between the transformer windings, for given primary and secondary Q's, so that two primary voltage humps of the required amplitude appear as the frequency is varied) the linearity and sensitivity of the discriminator can be very appreciably improved.

This statement, regarding linearity and sensitivity, refers, of course, to the relationship between voltage output and frequency-deviation from the central reference frequency (i.e. the nominal intermediate frequency).

Analysis of the phase discriminator for F-M applications has been made by K. R. Sturley (Refs. 27 and 28), and the results of this analysis will be used below It might be mentioned that a number of discriminator circuits for a wide variety of applications have been designed using the data derived by Sturley and very satisfactory results have been obtained in practice. Before proceeding to set out the design data, the circuit of Fig. 27.17 will be briefly discussed.

The voltages applied to the plates of the double diode valve V_2 will be E'_A and E'_B respectively. The output voltages from the diodes are developed across R_3 and R_4, and the circuit is arranged so that the available output voltage is equal to the **difference** between the two separate voltages. This means that when the frequency of the carrier voltage is exactly equal to the intermediate frequency, no output will be obtained from the detector. Reference to Fig. 27.16 should help to make this point quite clear, since the rectified voltages across R_3 and R_4 in Fig. 27.17 are given by the peak voltages applied to the diode plates multiplied by the detection efficiency of the diodes. As the signal deviates from the central reference frequency (i.e. the intermediate frequency), a voltage (E_{out}) will appear between the points P and N (Fig. 27.17), and its polarity will depend on the relative magnitudes of the voltages across R_3 and R_4; e.g. point P will be negative with respect to point N when the voltage across R_3 is less than that across R_4. It follows that it should be possible to calculate

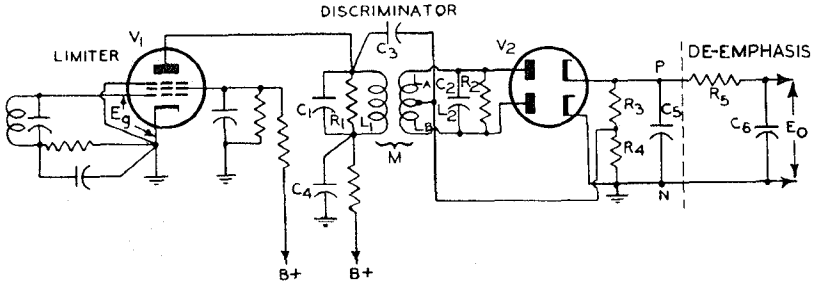


FIG 27·17 TYPICAL PHASE DISCRIMINATOR ARRANGEMENT FOR F-M DETECTION.

the relationship between output voltage and frequency change from

$$E_{out} = \eta(E'_A - E'_B) \tag{11}$$

where η = the diode detection efficiency, and is assumed to be the same for both diodes of V_2.

(B) Design data

For most designs it is usual to take the total secondary voltage E_2 as being twice the primary voltage E_1 i.e.

$$E_2/E_1 = 2. \tag{12}$$

Primary and secondary Q's are made equal, so that

$$Q = Q_1 = Q_2. \tag{13}$$

The value for Q is determined from

$$Q = f_r/(2\Delta f) \tag{14}$$

where f_r = intermediate frequency

and $2\Delta f$ = total frequency range for which substantially linear operation is required.

The coefficient of coupling for the transformer is found from

$$Qk = 1.5 \tag{15}$$

when a good compromise between sensitivity and linearity is required (the usual case).

For special cases where linearity is the main requirement it is suggested that

$$Qk = 2 \tag{16}$$

be used. The loss in sensitivity in this case is about 1.54 times as can be seen by comparing eqns. (20) and (21).

From the principles of coupled circuits it is possible to show that

$$\frac{E_2}{E_1} = Q_2 k \sqrt{\frac{L_2}{L_1}} \tag{17}$$

and for our particular cases with $E_2/E_1 = 2$ and $Qk = 1.5$ or 2, the relationship between L_2 and L_1 is

$$L_2/L_1 = 1.77 \text{ (for } Qk = 1.5) \tag{18}$$

and $$L_2/L_1 = 1 \text{ (for } Qk = 2). \tag{19}$$

The discriminator sensitivity at f_r is given by

$$S_{(Qk = 1.5)} = 5.465 \times 10^3 g_m Q^2 L_1 \eta E_g \text{ volts per kilocycle deviation,} \tag{20}$$

$$S_{(Qk = 2)} = 3.554 \times 10^3 g_m Q^2 L_1 \eta E_g \text{ volts per kilocycle deviation,} \tag{21}$$

where g_m = mutual conductance of V_1

Q = magnification factor determined from eqn. (14)

L_1 = primary inductance of transformer

η = diode detection efficiency

and E_g = peak voltage between grid and cathode of V_1.

It should be apparent that the sensitivity, given by eqns. (20) and (21), is directly proportional to E_g and so the output from the discriminator is dependent on the input voltage. To overcome this difficulty the valve V_1 is arranged as a limiter in such a way that the product $g_m E_g$ is kept almost constant, and thus the output voltage is no longer directly dependent on the magnitude of the signal input voltage.

Curves of discriminator output voltage versus frequency deviation can be found from vector diagrams similar to that of Fig. 27.16, and then introducing suitable cor-

rection factors to allow for variations in E_1 deliberately introduced by the transformer design. However, it is possible to determine two generalised curves for the design conditions previously imposed, one curve for $Qk = 1.5$ and the other for $Qk = 2$. The curves are shown in Fig. 27.18A, and relate the quantity X (which is a function of bandwidth) to the relative output voltage E_{rel}. Only the positive halves of the curves are shown since the negative halves have substantially the same shape. To determine the output voltage E_{out} against frequency, it is only necessary to multiply the horizontal scale by a factor determined by eqn. (14), and the vertical scale by a factor determined by eqn. (20) or eqn. (21) (depending on whether $Qk = 1.5$ or 2 is used).

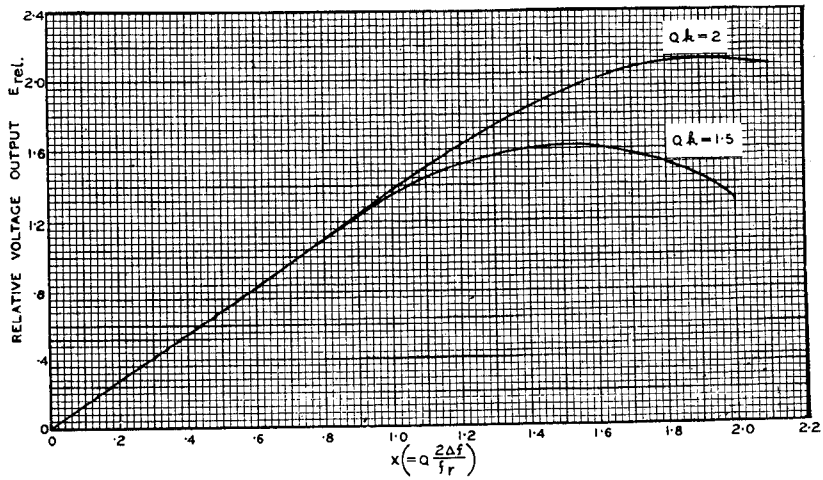


FIG. 27.18(A) GENERALISED PHASE DISCRIMINATOR CURVES OF RELATIVE VOLTAGE OUTPUT ($E_{rel.}$) VERSUS X WITH $E_2/E_1 = 2$; $Qk = 1.5$ AND 2.

The two curves shown in Fig. 27.18(A) are calculated from the following equations. For $Qk = 1.5$, the relative voltage output is

$$E_{rel} = \frac{3.25A}{\sqrt{(3.25 - X^2)^2 + 4X^2}} \tag{22}$$

and for $Qk = 2$,

$$E_{rel} = \frac{5A}{\sqrt{(5 - X^2)^2 + 4X^2}} \tag{23}$$

where $$A = \sqrt{1 + X^2}\left[\sqrt{\left(1 + \frac{X}{1 + X^2}\right)^2 + \left(\frac{1}{1 + X^2}\right)^2} - \sqrt{\left(1 - \frac{X}{1 + X^2}\right)^2 + \left(\frac{1}{1 + X^2}\right)^2}\right]$$

$X = Q\ 2\Delta f/f_r$

Q = magnification factor determined from eqn. (14). Equation (14) is the condition for $X = 1$

Δf = frequency deviation from f_r

and f_r = intermediate frequency.

To illustrate the design procedure, and to bring out additional points, a worked example is appended.

(C) Design example

A phase discriminator is required for use with a 10.7 Mc/s F-M i-f channel. The maximum frequency deviation of the carrier is $\pm$ 75 Kc/s. To make the problem

complete it will be taken that the highest audio frequency is 15 Kc/s and the de-emphasis time constant is 75 micro-seconds.

(a) The majority of applications call for reasonable discriminator sensitivity and so the condition $Qk = 1.5$ (see eqn. 15) is practically always used. Also, high primary dynamic impedance will increase the sensitivity of the discriminator. However, since Q is fixed by other considerations (see eqn. 14) L_1 should be large, but L_1 is limited by L_2 which in turn is limited by the permissible minimum secondary capacitance C_2. A value is selected for C_2 and the design can then proceed.

(b) A suitable value for C_2, including all strays, is 50 $\mu\mu$F. Then

$$L_2 = \frac{25\,330}{10.7^2 \times 50} = 4.41 \ \mu\text{H}.$$

From eqn. (18),

$$L_1 = \frac{L_2}{1.77} = \frac{4.41}{1.77} = 2.5 \ \mu\text{H}.$$

From this

$$C_1 = \frac{25\,330}{10.7^2 \times 2.5} = 88.5 \ \mu\mu\text{F (including all strays)}.$$

(c) If the discriminator frequency—voltage characteristic were exactly linear then it would be sufficient to make the total frequency range $2\Delta f = 2 \times 75 = 150$ Kc/s. To this would be added an allowance for frequency drift due to the oscillator and the discriminator tuned circuits. Since the discriminator characteristic is not exactly linear (it is linear for about 80% of the total curve using the data given as can be seen from Fig. 27.18) and the frequency drift is not always small it has become common practice in broadcast F-M circuits (of the type being considered) to make $2\Delta f$ from 200 to 400 Kc/s.

As a practical compromise we will take the total bandwidth ($2\Delta f$) as 250 Kc/s, but the design procedure is the same irrespective of what bandwidth is selected.

With $2\Delta f = 250$ Kc/s we have from eqn. (14)

$Q = 10.7/0.25 = 42.8$.

From eqn. (15), $Qk = 1.5$

and so $k = 1.5/42.8 = 0.035$.

(d) Summarizing, for the discriminator transformer (see also Fig. 27.17)

$L_1 = 2.5$ μH ; $L_2 = 4.41$ μH ; $C_1 = 88.5$ $\mu\mu$F ; $C_2 = 50$ $\mu\mu$F ; $Q = Q_1 = Q_2 = 42.8$; $k = 0.035$; $M = 0.116$ μH. Secondary winding to be centre-tapped. The capacitance values include all strays.

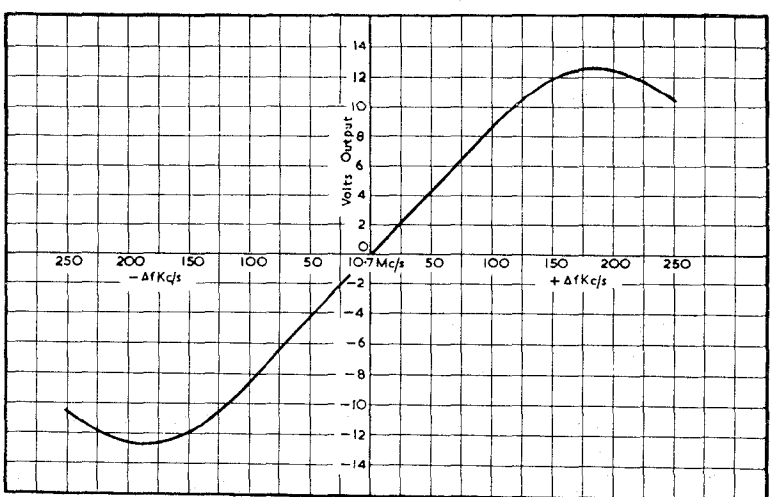


FIG. 27.18(B) Discriminator Characteristic Obtained From Design Example

(e) The discriminator sensitivity at f_r is given by eqn. (20). Assume $Eg = 1$ volt (peak), $g_m = 5$ mA/volt and $\eta = 0.7$. Then

$$S_{(Qk = 1.5)} = 5.465 \times 10^3 \times 5 \times 10^{-3} \times 42.8^2 \times 2.5 \times 10^{-6} \times 0.7 \times 1$$
$$= 0.0875 \text{ volts per kilocycle deviation.}$$

This also allows the vertical scale factor to be determined for the complete discriminator curve as shown on Fig. 27.18(B). The horizontal scale factor is found from

$$X = Q \frac{2\Delta f}{f_r} = 1 \text{ [i.e. eqn. (14)].}$$

Therefore $\Delta f = \dfrac{Xf_r}{2Q} = \dfrac{10.7 \times 10^3}{2 \times 42.8} = 125$ Kc/s.

The procedure for finding the plotted points on the curve of Fig. 27.18(B) is as follows. Draw up a table, as shown below, with values of X corresponding to values of E_{rel} read from the curve of Fig. 27.18(A). Since it has just been determined that $\Delta f = 125$ Kc/s when $X = 1$, the column for Δf can be filled in (e.g. when $X = 0.8$ then $\Delta f = 125 \times 0.8 = 100$ Kc/s, and so on). The sensitivity has been determined as 0.0875 volts per kilocycle deviation, and so for 25 Kc/s deviation $E_{out} = 0.0875 \times 25 = 2.19$ volts (the lowest deviation frequency in the table should be used to find E_{out} in this case). It is now seen that the value of $E_{out} = 2.19$ volts corresponds to $E_{rel} = 0.28$, and so the scale factor is $2.19/0.28 = 7.82$. If 7.82 is now multiplied by E_{rel} in each case, the column for E_{out} can be filled in. The complete curve for E_{out} versus Δf can now be plotted.

X	Δf	E_{rel}	E_{out}
0.2	25	0.28	2.19
0.4	50	0.56	4.38
0.6	75	0.84	6.56
0.8	100	1.12	8.76
1.0	125	1.36	10.61
1.2	150	1.52	11.9
1.4	175	1.6	12.5
1.5	187.5	1.62	12.7
1.6	200	1.6	12.5
1.8	225	1.52	11.9
2.0	250	1.31	10.5

(f) It now remains to determine suitable values for the other components in the circuit of Fig. 27.17.

C_3 is for the purpose of connecting the transformer primary to the secondary centre-tap, and providing isolation of the secondary from the h.t. on the plate of V_1. A suitable value is 100 $\mu\mu$F. The capacitor should have high insulation resistance.

C_4 is a by-pass capacitor ; a value of about 0.01 μF is usual.

R_3 and R_4 are made equal, and are generally about 100 000 ohms each.

C_5 acts as a by-pass for i-f but must not appreciably affect the audio frequency response. The usual value is about 100 $\mu\mu$F.

The de-emphasis network consists of R_5 and C_6. For 75 microsecond de-emphasis the nominal values would be 75 000 ohms and 0.001 μF respectively. If an improved a.c./d.c. ratio is thought to be necessary then suitable values would be say, 0.25 MΩ and 300 $\mu\mu$F. The grid resistor in the following a-f stage should not be less than 1 MΩ if excessive loss in gain is to be avoided. However, the actual values used in a receiver will generally deviate from these nominal figures if the overall audio frequency response of the receiver is made to follow the 75 microsecond de-emphasis curve to 15 Kc/s, because of the presence of stray capacitances etc. and in some cases to help compensate for the overall a-f response.

To determine R_1 :—the transformer primary damping due to a single diode circuit, connected as shown, is $R_{dc}/3$. For this circuit $R_{dc} = R_3 = R_4 = 100\,000$ ohms.

Also, because of the circuit arrangement, R_3 and R_4 are in parallel. The total damping, due to diode conduction currents in addition to R_3 and R_4, is then

$$\tfrac{1}{2}\left(\frac{R_{dc}}{3}\right) = \frac{100\,000}{6} = 16\,600\ \Omega.$$

If R_3 is not equal to R_4, the damping resistance is given by $R_3/3$ and $R_4/3$ in parallel i.e.

$R_3R_4/3(R_3 + R_4)$. (When $R_3 = R_4 = R_{dc}$ the value $R_{dc}/6$ is obtained as above).

Take the undamped primary Q (written as Q_u) as being 100, and neglect the additional damping due to the plate resistance of V_1. Then the total damping resistance (R) required to obtain a primary Q of 42.8 is

$$R = \frac{Q_uQ\omega L_1}{Q_u - Q} = \frac{100 \times 42.8 \times 2\pi \times 10.7 \times 2.5}{100 - 42.8}$$
$$= 12{,}500\ \Omega.$$

From this

$$R_1 = \frac{12\,500 \times 16\,600}{(16\,600 - 12\,500)} = 50\,600\ \Omega.$$

To determine R_2: The transformer secondary damping is given by

$R_3 = R_4 = R_{dc} = 100\,000\ \Omega$.

(This follows because the damping across each half of the secondary is $R_3/2$ and $R_4/2$ respectively, and in each case there is a step up, due to the transformer being centre tapped, of 4 times. From this, across the whole of the transformer secondary there are two resistances $4R_3/2$ and $4R_4/2$ in parallel, and since $R_3 = R_4 = R_{dc}$ the above result is obtained immediately).

The total damping resistance (R') required to make $Q_2 = Q_1 = 42.8$ is

$R' = 12\,500 \times 1.77 = 22\,100\ \Omega$.

From this

$$R_2 = \frac{22\,100 \times 100\,000}{(100\,000 - 22\,100)} = 28\,400\ \Omega.$$

The design of the limiter stage will be discussed in Chapter 29.

(g) Some causes of discriminator unbalance will be mentioned, before leaving this section, and it is helpful to consider the circuit as a bridge in which unbalance has to be eliminated. Even when the transformer secondary is centre-tapped accurately, unbalance can occur because the capacitive coupling between the two halves of the secondary winding and the primary winding is not necessarily equal. This calls for care in the method of arranging the windings. Two methods are in common use. The first uses a bifilar method with the two halves of the secondary wound side by side. The second method arranges the secondary into two halves, placed on either side of the primary winding, and the coupling of both sections, including that due to stray capacitances, is made equal.

Capacitive unbalance will also occur when the input capacitances of the diodes are not equal. Suitable arrangement of stray capacitances can often be used to help in offsetting this effect.

The use of a small capacitance connected across one of the diodes is helpful in reducing capacitive unbalance effects.

Balancing of the conduction resistances of the two diode units is largely outside the control of the receiver designer, but variation in the value of R_3 and R_4 can be made to assist in cases where a very high degree of balance is thought to be necessary. Additional precautions of this nature are seldom carried out in commercial receivers.

It should be noted in Fig. 27.17 that, if the resistors R_3 and R_4 are shunted by two separate capacitors, an additional series resistor or r-f choke will be required between the junction of R_3 and R_4 and the centre tap on L_2. Connecting the junction of R_3 and R_4 through a by-pass capacitor to ground would also effectively short-circuit the i-f primary voltage to ground, if the additional component is not used. For most circuits the arrangement shown is applicable, since it requires a minimum of components consistent with satisfactory performance. The alternative arrangement

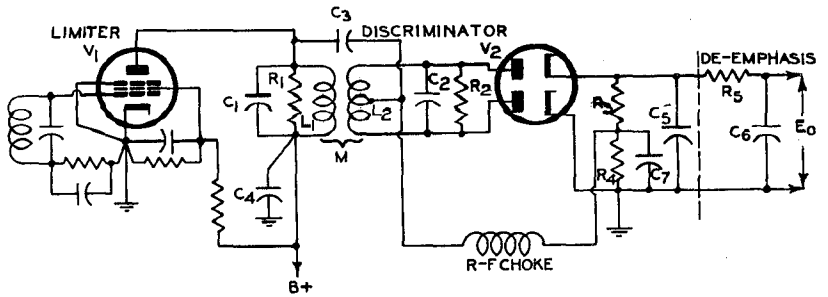


FIG. 27·19 ALTERNATIVE ARRANGEMENT FOR PHASE DISCRIMINATOR.

is shown in Fig. 27.19. The design procedure to be used is exactly as before, except that the primary circuit damping due to the diode circuits (the damping is actually across the r-f choke) will be approximately $R_{dc}/4$ instead of $R_{dc}/6$; the secondary circuit damping is R_{dc} as previously, where $R_{dc} = R_3 = R_4$. If a resistor is substituted for the r-f choke then the circuit damping is again modified depending on the value of resistance used in the circuit. Considerations leading to the choice of a suitable value for the inductance of the r-f choke will be given in detail in Chapter 29 Sect. 2, in connection with the discussion on a.f.c. discriminators.

It is perhaps worth mentioning that hum due to heater-cathode leakage is sometimes troublesome in discriminator circuits, particularly with miniature diodes, and a simple and effective cure for this trouble is to make the cathode positive with respect to the heater. This can be readily effected, for example in Fig. 27.19, by connecting a 10 000 Ω resistor by-passed by, say, a 0.01 μF mica capacitor between the earthy end of R_4 and ground ; the junction of R_4 and the 10 000 Ω resistor is then connected to B+ via a series resistor whose value is selected so that about 10 to 15 volts appears across the 10 000 Ω resistor (which now forms one arm of a voltage divider). In a typical case the series resistor would be about 0.16 MΩ for a B+ of 250 volts.

(iv) Ratio detectors

(A) General

Many of the details given below, regarding ratio detectors, have been taken from Refs. 34, 35 and 36. Practical experience with several of the arrangements shown has confirmed much of the data given in the design sections. However, a number of additional factors will warrant discussion.

The principle underlying many circuits for F-M detection is the peak rectification of two i-f voltages, the relative amplitudes of which are a function of frequency, together with means for combining the rectified voltages in reversed polarity. The output is then equal to the difference between the two rectified voltages. This statement is directly applicable to the phase discriminator circuits of Figs. 27.17 and 27.19, the two i-f voltages being those applied to the diode plates, and the rectified voltages combined in reversed polarity being those which appear across the load resistors R_3 and R_4. The way in which the two i-f voltages, applied to the diode plates, are dependent on the instantaneous intermediate frequency has been discussed in connection with Figs. 27.15 and 27.16. It was mentioned previously that, with the phase discriminator, changes in the magnitude of the input signal will give rise to amplitude changes in the resultant output voltage, and the need for some form of amplitude limiting was emphasized.

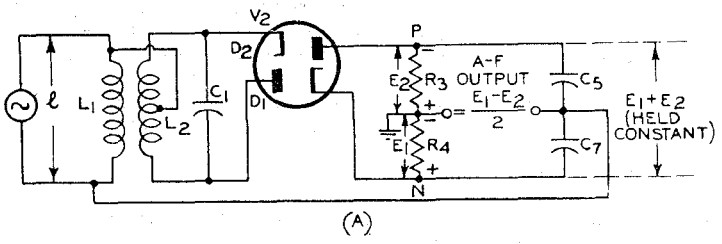
In an attempt to eliminate the necessity for a limiter, a ratio type of detector has been developed from the basic phase discriminator circuit. In this modified circuit the rectified voltages are split into two parts in such a way that their ratio is proportional to the ratio of the instantaneous i-f voltages applied to the detector diodes, and the sum of the two rectified voltages is kept constant. It has been found in this type of circuit that the useful output voltage, which is proportional to the difference between the two rectified voltages developed by the diode detectors, tends to be independent

of amplitude variations superimposed on a frequency modulated voltage applied to the discriminator circuit input terminals.

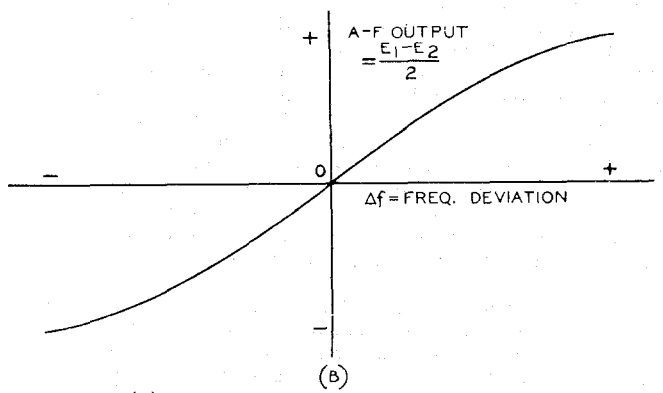
A basic ratio detector circuit is shown in Fig. 27.20(A). It can be seen that this is similar to the conventional phase discriminator but one of the diodes is reversed, and so the total voltage between the points P and N is equal to the **sum** of E_1 and E_2. The sum of E_1 and E_2 is held constant by means of a battery or a large capacitance. This point will be further discussed as we proceed. The audio output voltage is taken from the junction of R_3, R_4 and C_5, C_7 and is equal to $(E_1 - E_2)/2$. The voltage output with frequency change is seen from Fig. 27.20(B) to be similar to that for a conventional discriminator circuit.

The sum voltage $(E_1 + E_2)$ can be stabilized by using either a battery or by shunting a large capacitance across the load resistors R_3 and R_4. A battery would limit the operation in such a way that the input signal would need to be at least strong enough to overcome the fixed bias due to the battery voltage. A better solution is to use a capacitor, since the voltage across it will vary in proportion to the average signal amplitude and thus automatically adjust itself to the optimum operating level. This allows amplitude rejection to be secured for a wide range of input signal voltages, the lowest useful signal being determined by the ability of the diode rectifiers to conduct with small input voltages.

When a capacitor is used to stabilize the rectified output voltage its capacitance must be sufficiently large so that the sum of $E_1 + E_2$ cannot vary at an audio frequency rate. This calls for a time constant in the circuit made up from R_3, R_4 and the additional capacitance C of about 0.2 seconds. The effects of C_5 and C_7 on the time constant can be neglected, since the value of the capacitance C will be of the order of microfarads (usually about $8\mu F$).



(A)



(B)

FIG.27·20 (A) BASIC CIRCUIT OF RATIO DETECTOR.
(B) TYPICAL OUTPUT CURVE.

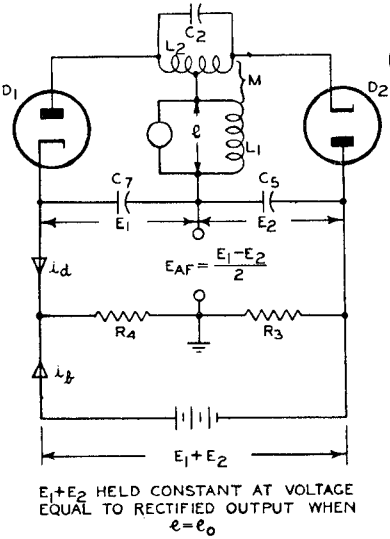


FIG. 27.21 RATIO DETECTOR CIRCUIT SHOWING CONDITIONS FOR DIFFERENT SIGNAL INPUT VOLTAGES.

It is worth noting that the a.v.c. voltages available from ratio detector circuits have values which are not always directly suitable for application to controlled stages. Some form of voltage divider arrangement is often necessary to obtain suitable voltages for securing the desired a.v.c. characteristic.

(B) Operation

A brief qualitative description of the operation of the ratio detector will be given here. A complete quantitative analysis has not been made, although many of the significant factors have been investigated (see Refs. 34, 35 and 36).

Fig. 27.21 shows the same basic circuit as Fig. 27.20(A), rearranged in a more convenient form for discussion. The main details of operation are also indicated, and show what happens in the circuit when the amplitude of the signal input voltage changes. For the case (A) where the amplitude of the signal input voltage is constant, the stabilizing current is zero and the circuit has essentially the same output characteristic as a phase discriminator. When the signal amplitude increases (B), the average diode current also increases, and resultant direct current flows into the stabilizing voltage source (i.e. the battery is being charged). From this since $E_1 + E_2$ remains constant, it is seen that the **effective** diode load resistance must decrease and so the primary and secondary circuits are more heavily damped than for the case (A) where the input voltage has a fixed value. The increased damping on the transformer circuits will tend to offset the increase in the amplitude of the input voltage, and so the output voltage will also tend to be constant.

Similarly, when the signal amplitude decreases—case (C)—the stabilizing voltage source supplies additional current (i.e. the battery is being discharged) to offset the reduction in diode current, so as to maintain $E_1 + E_2$ constant ; the effective diode load resistance is now increased, and so the circuit damping is reduced.

From this it is seen that stabilizing the rectified voltage results in the equivalent load resistance varying in such a way as to offset changes in the amplitude of the signal input voltage. It also follows that there must be optimum circuit conditions which will allow the undesired amplitude variations to be offset most effectively (although these conditions are not necessarily the same for all input voltages). The conditions for obtaining the most satisfactory operation will be summarized below when discussing the design of the ratio detector.

(C) Types of circuit

There are two types of ratio detector circuit in common use. The first of these is the so called balanced circuit and is illustrated by Fig. 27.22. At first glance this does not seem to be the same as the basic circuit previously discussed. However, if the tertiary winding is considered as L_1 for the moment (its presence will be explained presently), and it is taken that C_8 has a high reactance at audio frequencies and negligible reactance at i-f, then a simple re-arrangement of the circuit will show that it is the same as that of Figs. 27.20 and 27.21. Whether the junction of C_5 and C_7 is connected to ground, as shown in Fig. 27.22, or C_8 is connected from the junction of C_5 and C_7 to the junction of R_3 and R_4 as would be expected (since C_8 is part of the audio load circuit) is unimportant, as can be seen by redrawing the circuit. C is the stabilizing capacitor.

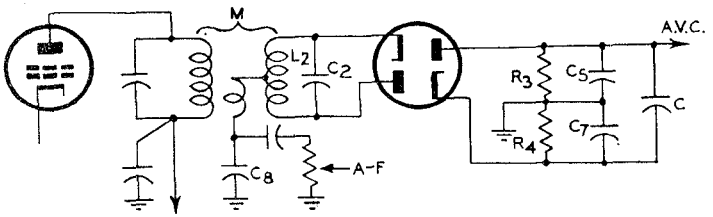


FIG. 27·22 BALANCED TYPE OF RATIO DETECTOR CIRCUIT.

The second type of circuit in common use is the unbalanced arrangement of Fig. 27.23. The operation is similar to the balanced arrangement but it obviously cannot be redrawn directly into a balanced arrangement. The A-M rejection is the same whether the centre-tap of R_3 and R_4 or any point along the load is grounded, provided that the stabilizing capacitor can hold the voltage across its terminals constant. This condition is not easily met, however, at very low audio frequencies because very long time constants for the diode load circuit have undesirable effects when the receiver is being tuned.

In general the balanced circuit will give better amplitude rejection at low frequencies than the unbalanced arrangement, when the time constants of the two circuits are the same.

Additional advantages of the balanced ratio detector are that the ratio of a.v.c. voltage to audio voltage is comparable with that obtained in conventional A-M detector circuits, and also a voltage is available which is zero at the centre frequency and can be used for a.f.c. purposes if so desired.

The presence of the tertiary winding in the discriminator transformer is readily understood when it is considered that it provides a simple method of tapping down on the transformer primary without the use of blocking capacitors and a choke, and at the same time allows the overall sensitivity of the detector to be increased by permitting a high primary circuit dynamic impedance. This is particularly helpful since the value of the total diode load resistance is generally small (usually less than 50 000 ohms total).

Because of the low value of load resistance it should be clear that high detection efficiencies are not easy to obtain, and so high perveance diodes are of considerable assistance in this regard because their internal impedance will be comparatively small. However, it is often found that high perveance diodes are more susceptible to hum pick-up than the medium perveance types and so are not necessarily the best choice in all circuits.

Before leaving this section an additional point of interest will be discussed. In Fig. 27.24 are shown typical curves of output voltage against signal input voltage for a ratio detector. It can be seen from these curves that the output is not constant with input voltage for a given frequency deviation. This effect can be offset to a large extent by using the valve preceding the ratio detector as a partial limiter. For weak signals the driver valve can be used as a straight voltage amplifier, but if a grid resistor and capacitor are included which have a fairly short time constant (say 10

microseconds or so) they can be used to derive a bias voltage for the grid of the valve when the signal exceeds some pre-determined level, and the valve can then be used to provide a degree of limiting. In this way the use of an additional valve is still avoided, since most ratio detectors operate satisfactorily with as little as 10 millivolts (or less) applied to the grid of the driver valve, but the advantages of additional amplitude limiting can be obtained on strong signals. Of course, satisfactory results are obtainable with a ratio detector alone and the application of a.v.c. bias to the earlier stages is helpful but improvement is possible with the arrangement suggested, and with very little additional trouble. With the partial limiter arrangement a.v.c. is sometimes applied to the first i-f voltage amplifier, the a.v.c. bias being derived from the ratio detector circuit as indicated in Figs. 27.22 and 27.23. Some receiver manufacturers do not use a.v.c. at all, but use suitable grid resistor-capacitor arrangements with both i-f valves to provide additional bias when the signal is sufficiently large. Some care is necessary with the limiter arrangements, since detuning of the i-f transformer can have adverse effects particularly with some types of noise interference. This point received consideration in Chapter 26 when the design of the F-M i-f transformers was being discussed.

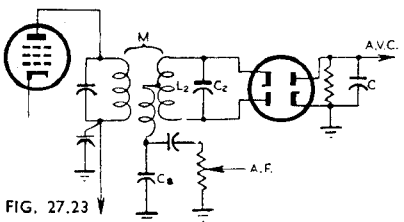


FIG. 27.23 Unbalanced Type of Ratio Detector

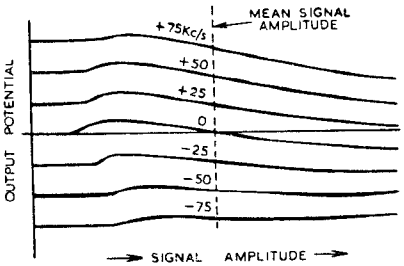


FIG. 27.24 Typical Input-Output Voltage Curves for Ratio Detector

(D) Design considerations

The data given below are quite general, but the circuit constants suggested are based on a centre frequency of about 10.7 Mc/s and a peak separation of approximately 350 Kc/s. Most of the information which follows (with certain modifications) is taken from Ref. 34, where a more detailed explanation is available.

Diode characteristics

Good ratio detector performance can be obtained with either high perveance diodes such as type 6AL5, or medium-perveance diodes such as type 6H6.

The circuits used will differ with high and medium perveance diodes in the extent to which the rectified output voltage is held constant. They will also differ with respect to the compensation used to minimize the residual unbalanced component of amplitude modulation in the output. The unbalance is brought about by secondary transformer detuning effects caused by input reactance variations due to the diodes. The magnitude of the effect is generally less for diodes having lower perveance.

Because the diode rectification efficiency, and hence the diode circuit loading, varies with signal level, optimum A-M rejection is obtained for a particular input voltage. The level at which optimum A-M rejection is obtained can be altered by varying the circuit constants, particularly the fraction of the total rectified voltage which is stabilized, or the ratio of secondary and tertiary voltages.

Secondary inductance

The secondary L/C ratio should be as high as possible consistent with circuit stability. This suggests capacitance values from 25-70 $\mu\mu$F. Also, the secondary Q should be as high as possible, depending on the required peak separation. Suitable Q values are 75 to 150, with the higher values giving improved sensitivity, for a given A-M rejection, but less peak separation.

Load resistors

The value R of the diode load resistors is generally selected to reduce the operating secondary circuit Q to a value of approximately one-fourth or less of its unloaded

value. Smaller values for R will increase the downward modulation handling capabilities of the detector, but will also reduce its sensitivity.

Primary L/C ratio and Q

The primary L/C ratio should be as large as possible to increase the sensitivity. The limiting factor is the maximum stable gain between the grid and plate of the ratio detector driver valve (i.e. the last i-f valve preceding the detector). When determining the maximum gain it should be remembered that the gain may increase during downward amplitude modulation, particularly on either side of the centre frequency.

If the primary Q is high enough so that the operating Q is determined mainly by the diode loading, the grid-plate gain will rise during the A-M cycle. This is advantageous since it increases the ability of the detector to reject downward modulation. The primary Q is made as high as possible consistent with peak separation and stable gain requirements.

Coupling

The value of coupling used, together with the number of turns in the tertiary winding, is the principal factor in determining the ratio of the tertiary voltage to the half secondary voltage. This ratio should always be close to unity. The coupling is generally adjusted to half critical in the actual circuit, since the degree of coupling is dependent on the other circuit component values and these are selected before the coupling is finally set to the desired amount.

Tertiary inductance

The number of turns on the tertiary winding is adjusted so that the required ratio of tertiary voltage to half secondary voltage is obtained (see under Coupling).

Reducing unbalanced A-M component

There will always be some residual amplitude modulation in the detector output because of the variation in the effective diode input capacitance during the A-M cycle, and because of the unbalance introduced by the transformer and other circuit components. Several methods are useful in overcoming this effect. One is to vary the effective centre-tap on the secondary winding (this method is shown in Fig. 27.26) and another is to make the resistors R_3 and R_4 shown in Fig. 27.25 unequal. In addition a resistor R_5 is used in series with the tertiary winding (see Fig. 27.25) to modify the peak diode currents, which has the effect of appreciably reducing the unbalanced A-M component particularly at high input voltages. The methods using resistors to reduce unbalance also reduce the detector sensitivity.

The reduction of unbalance effects is carried out by observing the condition for minimum A-M output when a signal which is simultaneously amplitude and frequency modulated is applied to the detector.

Time constant of stabilizing voltage

The discharge time constant of the stabilizing capacitance and the load resistance should be about 0.2 second. Larger time constants will give better amplitude rejection when the undesired modulating frequency is low, but have undesirable effects on the tuning. The tuning effect is similar to that given by an ordinary A-M receiver when the a.v.c. time constant is too long.

Experiments with the time constant of this circuit give some interesting effects. If the stabilizing capacitance is made very large, say 100 μF or so, and the receiver is tuned rapidly across a signal, it will be found that the point of maximum output is very easily determined, and there is no effect from the usual side responses. When the receiver is detuned the noise level rises, as the capacitor discharges, and the side responses again become evident until the receiver has been tuned once through the point of maximum output.

Additional details

It is not particularly easy to achieve a good balance with the ratio detector circuit, and usually more care is required in this respect than with the conventional phase discriminator. However, the better the balance obtained the better will be the rejection of undesired amplitude modulation.

Although the side responses are normally well down on the response at the main tuning point, with this type of circuit, considerable improvement has been noticed

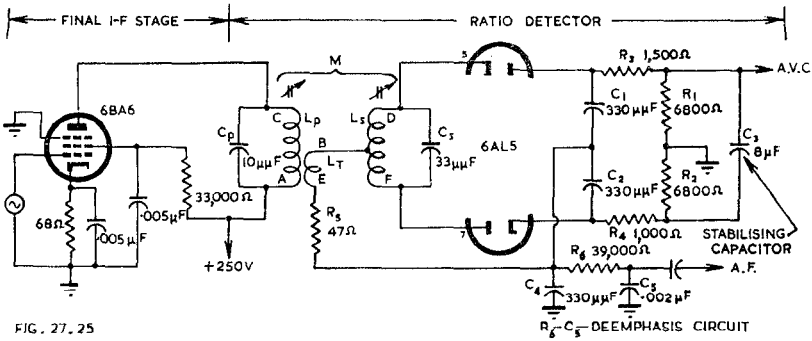


FIG. 27.25

when the bandwidth of the discriminator is fairly large (say 300 to 400 Kc/s) and the i-f response is such as to give steep sides to the overall selectivity curve. With receivers using two i-f transformers (each critically-coupled and both having primary and secondary Q's of about 75) the side responses are still sufficiently large to be noticeable, although they are 12-15 db down on the main tuning position. Receivers using three transformers (each critically-coupled and having Q's of about 70) give a very marked improvement, and the two undesired side responses can only be found after careful searching. If the transformers are made more selective the side responses are reduced, but the additional non-linear distortion introduced by the tuned circuits may no longer be negligible, as can be determined from the data given in Chapter 26. Further, the amount of amplitude modulation on a carrier goes up as the selectivity of the transformers is increased, and this undesired A-M has to be removed by the ratio detector thereby reducing its effectiveness to other undesired external noise. Even in the case of the receiver with only two i-f transformers, the undesired side responses are very much less noticeable than with receivers using the usual limiter and discriminator combination

(E) Practical circuits

Two circuits which have been constructed and tested under working conditions are shown in Figs. 27.25 and 27.26. The intermediate frequency is 10.7 Mc/s Constructional details and performance data can be found in Refs. 34 and 37.

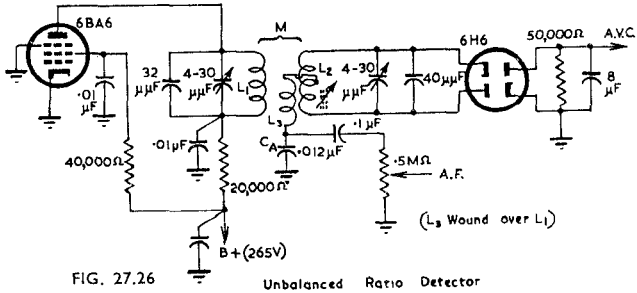


FIG. 27.26 Unbalanced Ratio Detector

De-emphasis is obtained in the circuit of Fig. 27.26 by adjusting the value of the capacitor marked C_4. The time constant (0.4 second) of the diode load circuit is about twice as long as that previously recommended for typical cases, but the performance is quite good, and, as suggested in Ref. 37, the individual designer can set the constants to suit his own requirements.

The secondary winding for the circuit of Fig. 27.25 is a bifilar arrangement, while that of Fig. 27.26 has the secondary split into two sections placed on either side of the primary. In the latter case slug tuning is used for one half of the secondary so that the effective centre tap can be set to any desired position.

(F) Measurements on ratio detectors

Primary and secondary *Q*'s

To measure the unloaded primary Q, the double diode valve is removed from its socket and the secondary is detuned. The primary Q is then determined by the selectivity of the primary tuned circuit. The loaded primary Q is measured in the same way but with the double-diode valve in the circuit.

To measure the secondary Q the primary is heavily loaded by a shunt resistor. The secondary Q is then determined from the selectivity of the secondary winding as indicated by the rectified voltage variation with frequency. When measuring the unloaded secondary Q, the diode load resistance should be replaced by a resistance of about one megohm. When measuring the loaded secondary Q, the normal load resistors should be used. For these measurements the centre-tap of the secondary winding should be disconnected from the tertiary winding, to prevent the tertiary voltage from contributing to the rectified voltage.

Coupling

The percentage of critical-coupling can be measured by noting the change in primary voltage as the secondary is varied from a tuned to a detuned condition. With all circuit conditions normal, and the signal input voltage set to the intermediate frequency, the primary voltage (E_1) is noted. With the same input signal level, the secondary is detuned so that the primary voltage rises to E_2. The percentage of critical-coupling can then be expressed in terms of the ratio between the primary voltage with the secondary detuned and tuned using the relationship

$$\frac{k}{k_{crit}} = \sqrt{\frac{E_2}{E_1} - 1}.$$

For example, if the signal voltage at the plate rises 25 per cent. (i.e. $E_2 = 1.25\ E_1$) when the secondary is detuned, the coupling is 50 per cent of critical.

The ratio between the secondary and tertiary voltages can be measured indirectly in terms of the rectified output voltage which is obtained (a) with the secondary tuned and (b) with the secondary detuned. In both cases the input signal is adjusted so that the primary voltage remains constant. If the ratio between the voltages read in (a) and (b) is r, that is if

$$r = \frac{\text{Rectified voltage (tuned secondary)}}{\text{Rectified voltage (detuned secondary)}}$$

then $$\frac{S}{P} = \sqrt{r^2 - 1}$$

where S = half secondary voltage at centre frequency

P = "primary" (i.e. tertiary) voltage effective in the diode circuit at the centre frequency.

The ratio S/P is usually made equal to unity.

Signal generator

It is convenient to have available a signal generator of good quality capable of being simultaneously frequency and amplitude modulated. Undesired amplitude and frequency modulation should not be present in the generator output.

Alignment procedure

The ratio detector may be aligned by using either an unmodulated signal set to the centre frequency and a d.c. vacuum-tube voltmeter, or by using a F-M signal generator and an oscillograph.

If an unmodulated signal generator is used, the procedure is to set the signal to the intermediate frequency, and with the d.c. vacuum-tube voltmeter connected to measure the rectified output voltage (this is usually the a.v.c. take-off point), the primary tuning being adjusted for maximum voltage output.

The procedure used for adjusting the secondary tuning depends upon whether the centre-tap of the stabilizing voltage is earthed or whether one end is earthed. If the centre-tap is earthed, the secondary tuning is adjusted so that the d.c. voltage at the audio take-off point is equal to zero ; the d.c. vacuum-tube voltmeter is shifted to the audio take-off point for this measurement. If the detector is of the unbalanced

type the secondary tuning is adjusted so that the d.c. voltage at the audio take-off point is equal to half the total rectified voltage. As an alternative an amplitude modulated signal can be used, the primary trimmer is adjusted for maximum d.c. output voltage and the secondary trimmer adjusted to give minimum audio output; the residual output is measured in the conventional manner. Circuit unbalance is indicated if the two methods do not give the same secondary trimmer setting.

If sweep alignment is used, the primary can be accurately aligned by using a comparatively low deviation, and adjusting the primary trimmer for the maximum amplitude of output voltage. The secondary may be adjusted by using a deviation such that the total frequency swing (twice the deviation) is equal to the peak separation. This procedure makes it possible to adjust the secondary tuning so that a symmetrical detector characteristic is obtained.

Peak separation

The separation between the peaks on the F-M output characteristic of a ratio detector may be measured by applying a frequency modulated signal and increasing the deviation until the response is just observed to flatten at the peaks. When this is done, the peak separation is equal to twice the deviation.

If an attempt is made to measure the peak separation by plotting the output characteristic point by point, the peak separation obtained will usually be considerably less than that obtained under dynamic conditions with the output voltage stabilized. The F-M detector characteristic may be plotted point by point provided a battery of the proper voltage is connected across the stabilizing capacitor. The voltage of this battery must be equal to the rectified voltage which exists at the centre frequency. In practice it is convenient to use a 7.5 volt " C " battery and to adjust the signal input so that the capacitor-stabilized voltage at the centre frequency is equal to the battery voltage.

It is worth noting that the peak separation is not constant for all values of input voltage, and measurements should be made for several representative voltages of the magnitude likely to be encountered under practical conditions of reception. The peak separation is wider for larger input voltages, as a result of the increased diode loading on the tuned circuits. Similarly the peak separation is less for smaller input voltages because of reduced circuit damping.

Measurement of A-M rejection

The measurement of A-M rejection can be carried out using a signal generator which can be simultaneously frequency and amplitude modulated.

Ref. 34 shows a number of the typical wedge-shaped patterns which are obtained when visual methods are used for determining the amplitude modulation present in the audio output. A pattern of the type to be expected is shown in Fig. 27.27.

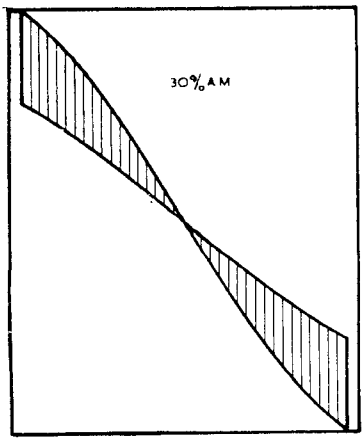


FIG. 27.27

The measurement of the A-M rejection of a ratio detector can be described in terms of the pattern obtained for a given frequency deviation and a given percentage of amplitude modulation.

The measurements should be made for several different values of input voltage. Ideally the pattern obtained should be a diagonal line regardless of the presence of amplitude modulation. The amount by which the pattern departs from a straight line indicates the extent to which the detector fails to reject amplitude modulation.

To measure A-M rejection with a generator which can only be frequency modulated the procedure is as follows. A frequency modulated signal fully deviated (± 75 Kc/s

in the usual case) is applied, and a battery of which the voltage is equal to the rectified output is shunted across the stabilizing capacitor. The magnitude of the input signal is now reduced until the output becomes distorted as a result of the diodes being biased by the stabilizing voltage, and finally the F-M output drops to zero. The ratio between the initial input signal and the minimum input signal for which the F-M output becomes distorted is then a measure of the amount of downward modulation that the detector can reject. For example if the voltage ratio is r, then the percentage of downward amplitude modulation which can be handled is $100\ (r - 1)/r$. To determine the rejection of the detector for upward amplitude modulation the same set-up is used and the change in output is noted as the input signal is increased. Since the amplitude of the input signal is not varied dynamically, this method will not indicate any unbalanced component which may be present in the output. The latter is more conveniently measured using simultaneous F-M and A-M as discussed previously.

Another method which can be applied to measure the amplitude rejection properties of **any** type of detector for different signal input voltages may be worth discussing. The input signal is simultaneously frequency and amplitude modulated. Any audio modulating frequencies can be selected which are not harmonically related, and suitable values are say 400 c/s for F-M and 30 c/s for A-M. The percentage A-M can be taken as 30% (or any value desired) and the deviation as $\pm$ 22.5 Kc/s (or any other value). The ratio of the desired and undesired audio outputs can then be measured on a frequency selective voltmeter such as a wave analyser. Measurements can be made at the centre frequency to indicate residual A-M, and for various frequencies off the centre frequency to determine the rejection capabilities of the detection system under operating conditions ; e.g. those which occur when oscillator and other frequency drift occurs. Low audio frequencies are preferable for this test (and also for the previous methods), particularly with ratio detectors, since the amplitude rejection is least for this condition. Tests on a number of ratio detectors have indicated similar performance when high audio modulating frequencies are used, but considerable variation occurs in the amount of amplitude rejection obtained for the lower audio frequencies using balanced and unbalanced circuits. This is readily understood when the function of the stabilizing capacitor is considered.

Standard test procedures have been devised for F-M receivers, and standard methods for evaluating the degree of A-M rejection, downward modulation handling capability, and the effects of mistuning are described in Chapter 37.

Non-linear distortion

Distortion measurements are usually quite difficult to carry out with any degree of accuracy because of the inherent non-linear distortion present in the signal source and test equipment. Tests on typical F-M receivers using limiter-discriminator combinations and ratio detectors have been made, using the low power stages of a F-M broadcast transmitter as the signal source. The non-linear distortion in the transmitter signal was less than 0.5% for frequencies from 100 c/s to 15 Kc/s, and less than 1% from 30 to 100 c/s ; the frequency deviation was set to $\pm$ 75 Kc/s in all cases.

Both types of receiver indicated a measured overall distortion of the order of 2 to 2.5% in the frequency range 100 c/s to 7.5 Kc/s, 3 to 5% at 50 c/s and 5% at 15 Kc/s although this latter case was a visual check only. Above 10 Kc/s the non-linear distortion with ratio detector receivers is generally somewhat higher than with limiter-discriminator receivers. The input in all cases was approximately 100 μV and the output was adjusted to 0.5 watt. The test frequency was 97.2 Mc/s and the i-f of all receivers was 10.7 Mc/s. The measured distortion for the a-f amplifier alone was 0.5% for the range 100 c/s to 7.5 Kc/s and 2% at 50 c/s ; above 7.5 Kc/s, observation was made using an oscillograph and as there was no visible distortion it was assumed that distortion was less than 3%.

The non-linear distortion is increased with ratio detector receivers when the magnitude of the input voltage is made very large. With the other type of receiver the input signal must be sufficiently large to ensure satisfactory limiter operation. Receivers

using a combination of partial limiting and a ratio detector give excellent results for a wide range of signal input voltages, and do not require extra valves.

The test conditions used are very severe, as it is unlikely that a 15 Kc/s audio signal will cause 75 Kc/s deviation ; although it should not be overlooked that pre-emphasis in the transmitter will cause a 15 Kc/s modulating signal to be increased in magnitude by about 17 db. Listening tests indicate that excellent results are obtainable with any of the receiver arrangements. It will be appreciated that the possibility of errors in the distortion measurements are very large, and the results are given to serve as an indication of the magnitude of the distortion to be expected with typical F-M receivers which do not include elaborate design features, but conform to good engineering practice.

SECTION 3 : AUTOMATIC VOLUME CONTROL

(i) Introduction (ii) Simple a.v.c. (iii) Delayed a.v.c. (iv) Methods of feed (a) Series feed (b) Parallel feed (v) Typical circuits (vi) A.V.C. application (vii) Amplified a.v.c. (viii) Audio a.v.c. (ix) Modulation rise (x) A.V.C. with battery valves (xi) Special case with simple a.v.c. (xii) The a.v.c. filter and its time constants (xiii) A.V.C. characteristics (xiv) An improved form of a.v.c. characteristic (xv) Design methods.

(i) Introduction

Automatic volume control is a device which automatically varies the total amplification of the signal in a radio receiver with changing strength of the received signal carrier wave. In practice the usual arrangement is to employ valves having " remote cut-off " or " variable-mu " grids and to apply to them a bias which is a function of the strength of the carrier.

From the definition given, it would be correctly inferred that a more exact term to describe the system would be automatic gain control (a.g.c.). The older term a.v.c. has been retained here as the name is not likely to lead to any confusion, and is widely used throughout the radio industry.

(ii) Simple a.v.c.

In order to obtain simple a.v.c. it is only necessary to add resistor R_4 and capacitor C_4 to the ordinary diode detector circuit shown in Fig. 27.28. In any diode detector there is developed across the load resistor (R_1 and R_2 in series) a voltage which is proportional to the strength of the carrier voltage at the diode. The diode plate end of the load resistor is negative with respect to earth (Fig. 27.28) and therefore a negative a.v.c. voltage is applied to the controlled grids. R_4 and C_4 form a filter to remove the a-f component and any residual i-f and leave only the direct component of voltage.

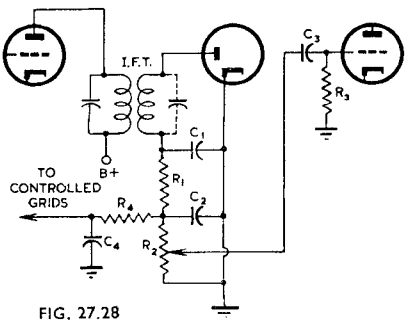


FIG. 27.28

Since a capacitor in series with a resistor takes a finite time to charge or discharge, the a.v.c. filter circuit has a " time constant." The time constant of R_4 and C_4 is equal to R_4C_4. For example, if R_4 is 1 megohm and C_4 is 0.25 microfarad the time constant will be 0.25 second. In this circuit the time constant is also influenced by R_1 during charge and by R_2 during discharge, but since R_1 is small compared with R_4 it will be sufficiently close for practical purposes to regard R_4C_4 as giving the time

constant during charge, and $C_4(R_4 + R_2)$ as the time constant during discharge. It is seen that the charge time constant is shorter than the discharge time constant. Time constants in a.v.c. circuits will be discussed in detail in (xii) below.

For 100% rectification efficiency the a.v.c. voltage would equal the peak i-f voltage applied to the diode. Because of losses the a.v.c. voltage is always somewhat less than the peak carrier voltage (this is readily seen from Figs. 27.5 and 27.6), and since, in general, a higher voltage is required for the a.v.c. than for detection, this will be a limitation to the use of simple a.v.c.

The design of the i-f transformer to couple the i-f voltage into the diode circuit is quite straightforward. The damping to be expected across the windings due to the diode circuits has already been discussed in Sect. 1(i)Cc of this chapter. Methods of i-f transformer design are detailed in Chapter 26.

In the circuit of Fig. 27.28 the d.c. diode load consists of R_1 and R_2 in series, R_1 being used in conjunction with capacitors C_1 and C_2 to form a filter to prevent the major part of the undesired i-f voltages from appearing across R_2. The volume control is R_2 in this circuit, and the advantages and disadvantages of using the control in this position were discussed in Sect. 1(i)Dc above. At audio frequencies R_2 is shunted by R_4 and by R_3 when the setting for R_2 is at the maximum. It follows that the diode load for a.c. is considerably different from that for d.c., and, as previously discussed in Sect. 1(i), considerable non-linear distortion of the a-f output will result when the modulation percentage is high. R_4 and C_4 will substantially remove all audio frequency variations from the a.v.c. bias applied to the controlled stages, as well as any residual i-f voltages which may be present across R_2.

Fig. 27.28 shows R_4 connected to the junction of R_1 and R_2, but in some cases R_4 is connected to the top of R_1. This latter arrangement will give a slightly higher a.v.c. voltage, the amount depending on the size of R_1, but the amount of i-f filtering for the controlled stages is reduced. With the usual component values it is not very important which arrangement is used.

Owing to the effects of contact potential in the diode, together with rectification due to unavoidable noise voltages, there is a voltage developed across R_2 even with no carrier input. Even with a weak carrier input this voltage is increased. Consequently it will be seen that with the weakest carrier likely to be received there is an appreciable negative voltage applied to the controlled grids. If no means were taken to compensate for this, the overall sensitivity of the receiver would be decreased. Compensation for the initial standing bias, before a carrier is received, can be carried out by applying a lower minimum negative bias to the controlled stages. However, a very real disadvantage of simple a.v.c. is now apparent in that the sensitivity of the receiver may decrease as soon as a carrier is received. To overcome the loss in sensitivity on weak signals a delayed a.v.c. system is used and this gives very much improved control.

A special case of the effects of contact potential with zero bias valves is worth noting before leaving this section. Suppose a negative bias voltage exists between the grids and cathodes of the controlled valves due to positive grid current. This current can be sufficiently large to cause an appreciable negative bias voltage to appear across the resistance common to the controlled stages and the detector, and so give rise to a negative bias voltage between plate and cathode of the diode. Under this condition, if simple a.v.c. is being used, there will be no output from the receiver until the signal is sufficiently large to overcome this delay bias on the detector. If a separate diode is used for a.v.c. the effect will be to increase the delay bias. Typical examples of the effect have occurred in practice with type 1P5-GT voltage amplifiers used in conjunction with the diode section of a type 1H5-GT. An obvious remedy is to apply a small positive bias voltage to the diode plate, but the grid current can often be appreciably reduced by increasing the screen voltage.

(iii) Delayed a.v.c.

The " delay " in delayed a.v.c. refers to voltage delay, not time delay. A delayed a.v.c. system is one which does not come into operation (i.e. it is delayed) until the

carrier strength reaches a pre-determined level. The result is that no a.v.c. voltage is applied to the grids of the controlled stages until a certain carrier strength is reached, and the receiver will have its maximum sensitivity for signals with an amplitude below this pre-determined level.

The circuit used for delayed a.v.c. also makes possible improved rectification efficiency in the a.v.c. circuit, thus producing slightly greater a.v.c. voltage for the same peak diode voltage. This is due to the higher value of a.v.c. diode load resistance (R_7 in Fig. 27.29) permissible in this circuit. With the a.v.c. arrangement shown the a.c. loading on the detector circuit is reduced when compared with the arrangement of Fig. 27.28 and this reduces the distortion of the audio output voltage. Some non-linear distortion of the modulation envelope does occur at the primary of the transformer but this is considerably less than that introduced when the a.v.c. voltage is obtained from the secondary circuit. In addition, the overall selectivity up to the primary of the i-f transformer is less than that at the secondary, and the a.v.c. will start to operate further from the carrier frequency than if fed from the secondary. The advantage here is that the tendency to give shrill reproduction is reduced as the receiver is detuned from a carrier.

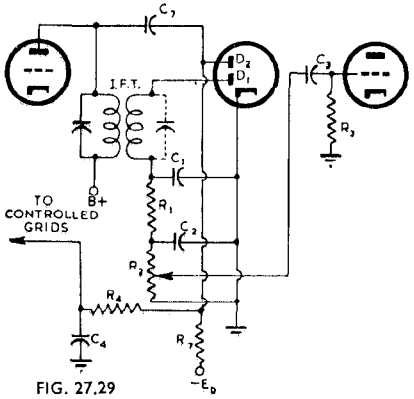


FIG. 27.29

Differential distortion, caused by variable damping of the a.v.c. diode input circuit, is frequently mentioned as an inherent disadvantage of delayed a.v.c. because of the distortion which is introduced when the diode bias line cuts the modulation envelope. Careful measurements have shown that the additional distortion occurring just as the a.v.c. diode starts to conduct is quite small provided that the delay voltage is small and the average depth of modulation is not large (say 50% or so). With a delay voltage (E_D, Fig. 27.29) of 3 volts the total harmonic distortion was found to increase from an average level of about 2.5% to a peak of 4%. Not only is the amount of distortion fairly small, with the usual depth of modulation, but it only occurs over a limited range of input signals, which, with a small delay voltage such as 3 volts or less, occurs at such weak signal strengths as to be relatively unimportant. However with 100% modulation this type of distortion will always occur. Of course, when the input voltage is too small for the a.v.c. diode to conduct there is no distortion. From the evidence available, it appears that the effect of differential distortion is a comparatively minor one when the circuit is correctly designed, and a small delay voltage is used. Detailed discussion of the distortion produced by delayed a.v.c. can be found in Refs. 44 (p. 189) and 46.

If it is desired to apply full a.v.c. voltage to certain controlled stages and a fractional part only to another stage, this may be done by tapping R_7 at a suitable point and by adding a filter circuit similar to that made up from R_4 and C_4.

Staggering* of the a.v.c. is sometimes advantageous, as a considerable improvement in signal-to-noise ratio is often possible by controlling mainly the i-f amplifier valves.

*By staggering of the a.v.c. is meant the application of different values of a.v.c. voltage to various stages

However, in some cases this leads to difficulties with cross modulation. When cross modulation is a serious problem it is preferable to control the r-f amplifier valves fully. Often no great care is taken with broadcast receivers in the method of applying a.v.c. With high quality communications receivers precautions are necessary, and it is helpful if the r-f and i-f valves to be controlled by a.v.c. can be selected by the operator. In this way optimum performance can be obtained under all conditions. The usual arrangement, however, is to design an a.v.c. system with compromise characteristics and fit manual switching for the selection of suitable time constants. The signal-to-noise ratio of the receiver should be measured when the a.v.c. characteristic is being determined, to ensure that the performance of the receiver is not seriously impaired when the signal input voltage is increased. Cross modulation tests are also necessary when the receiver performance is being determined. Further discussion of these problems can be found in Ref. 43 (pages 169 and 179). A dual a.v.c. system which has interesting possibilities is described in Ref. 50. Further discussion on a.v.c. and noise is given in Chapter 35 Sect. 3(i).

When a duo-diode triode (or pentode) valve is used with cathode bias, the value of the bias is usually between 2 and 3 volts. Such a voltage is suitable for use as a.v.c. delay bias ; a very simple arrangement is possible by returning R_7 to earth as shown in Fig. 27.34. Alteration of the delay bias because of the presence of contact potentials must be considered, and this effect has already been discussed in (ii) above.

A circuit which eliminates differential distortion, even with large delay voltages and high modulation levels, is shown in Fig. 27.38B. Signal detection and a.v.c. detection are carried out as before, but a diode, D_3, and the three resistors R_8, R_9 and R_{10} are also used. R_9 and R_{10} form a voltage divider from B+ to ground, the junction of these resistors and R_8 having a potential of, say, +50 volts. Typical values for R_4 and R_8 could be 1 megohm and 5 megohms respectively, and it will be seen that R_4 and R_8 form a voltage divider between +50 volts and the source of a.v.c. potential.

The operation of the circuit can be explained most simply if the diode D_3 is ignored initially. Under these conditions, with no signal input to the receiver, point X will be practically at ground potential since there will be no i-f input to the diode D_2 and the voltage at Y will be approximately

$$+ 50 \times \frac{R_4}{R_4 + R_8} = + 8\text{-}1/3 \text{ volts.}$$

Now as an increasing signal is applied to the input of the receiver, the available a.v.c. voltage at X will increase, and when this voltage reaches −10 volts, the potential across the voltage divider R_4R_8 will be 50 − (−10) volts, and the potential at Y will be

$$-10 + (50 + 10) \frac{R_4}{R_4 + R_8} = 0 \text{ volts.}$$

A still larger voltage of −40 volts at X will give at Y

$$-40 + (50 + 40) \frac{R_4}{R_4 + R_8} = -25 \text{ volts}$$

Thus in the absence of the diode D_3, point Y would have a potential with respect to ground which was positive in the absence of a signal and became less positive, zero and then more negative progressively as the signal input increased.

However the diode D_3 modifies this voltage variation by conducting whenever point Y tends to become positive. The result is that under no signal and small signal conditions point Y, from which a.v.c. is applied, is substantially at ground potential but as the signal input increases above some critical value, Y becomes progressively more negative. Thus the requirements of delayed a.v.c. have been met, although the loading of the diode D_2 on the primary tuned circuit is near enough to being constant whether a.v.c. is being applied or not.

After the delay has been overcome, the increase in negative potential at Y is not so rapid as the increase at X, the ratio being the same as that of the voltage divider formed

by R_4 and R_8. However by using a large value of resistance for R_8 and a high positive voltage the ratio can be made as close to unity as required by any practical considerations.

The cost of the resistors R_9 and R_{10} can often be avoided by using a source such as the screen of a valve which has no a.v.c. applied, or a voltage divider used for some other purpose, for the positive potential. To save the cost of a valve having an additional diode for D_3 it is quite possible to use the signal diode D_1 as the source of a.v.c. voltages, and D_2 as the " sinking " diode. Alternatively D_1 and D_2 can be used as in Fig. 27.38B and the suppressor grid of say the i-f amplifier can be used as D_3, although in this case with no signal applied the a.v.c. line will take up the potential of the cathode of the i-f valve.

This method of providing delay either to the first stages or to all controlled stages of a receiver is of course equally applicable whether manual or automatic volume control is used

(iv) Methods of feed

The a.v.c. voltage may be fed through the secondary of the r.f. transformer to the grid of the valve (sometimes called " Series Feed ") or directly to the grid (sometimes called " Shunt or Parallel Feed "). In the latter case it is necessary to use a blocking capacitor between the top of the tuned circuit and the grid to avoid short-circuiting the a.v.c. voltage to ground through the comparatively low resistance of the tuned-circuit inductor. Actually the second term is a misnomer, since either circuit arrangement leads to the r-f and d.c. bias voltages being applied, effectively, in series with one another between grid and cathode of the controlled valve. This may not be immediately obvious in the case of so called " parallel feed," but can be readily seen by drawing an equivalent circuit consisting of a r-f voltage generator in series with a capacitor and in parallel with these a resistor in series with a battery. The capacitor charges to some value q because of the battery, and the r-f voltage due to the generator then acts in series with the resultant voltage across the capacitor, varying the total charge and consequently the voltage across the output terminals of the circuit.

It should be noted that the terms " Series Feed " and " Parallel Feed " have no bearing on the type of a.v.c. filter circuit, which may be series, parallel or a combination of both. The two types of a.v.c. feed circuits will now be considered in greater detail.

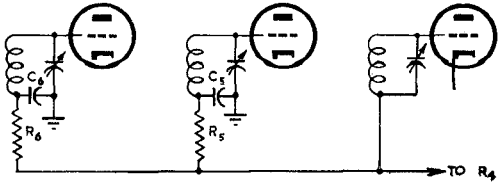


FIG. 27.30

(a) Series feed

One arrangement of series feed is shown in Fig. 27.30. It will be seen that in each r-f tuned circuit a blocking capacitor (C_5, C_6) is used so that the rotor of the ganged tuning capacitors may be earthed and the a.v.c. voltage fed to the lower ends of the coils. In the r-f stages the use of this blocking capacitor will reduce the frequency coverage, and may also affect the tracking of the tuned circuits. To reduce these effects the same capacitance value should be used in each of the r-f stages, and the value selected should be fairly large consistent with other considerations. Also, if the capacitors are not to affect the Q of the tuned circuits adversely, they must be of a low loss type. A disadvantage of a high capacitance is that it increases the time constant of the a.v.c. circuit.

For typical cases C_5 and C_6 would be about 0.05 μF if the maximum capacitance of the tuning capacitor is about 400 $\mu\mu$F. The effect on the tuning range is easily

determined by considering the reduction in total capacitance due to the capacitors being connected in series. Resistors R_5 and R_6 are used in conjunction with the capacitors to provide decoupling between the various stages ; typical resistance values are 100 000 ohms.

Since the tuning capacitors in i-f transformers need not be connected directly to earth, blocking capacitors are not necessary. In these circuits the capacitor C_4 (Fig. 27.29) serves to by-pass all high-frequency components of current from the earthy sides of the secondaries of the tuned circuits of the i.f stages to earth, as well as being part of the a.v.c. filter.

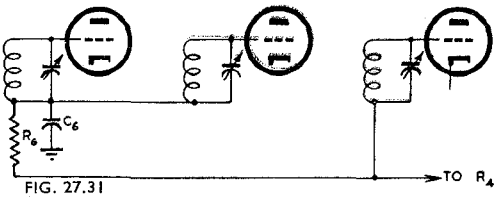


FIG. 27.31

With the r.f. stages an alternative arrangement is to insulate the rotor of the ganged capacitors, and to by-pass it to earth by a single capacitor (C_6, Fig. 27.31). This enables the a.v.c. voltage to be applied without using any blocking capacitors in the r-f tuned circuits, and has the further advantage that the time constant of the a.v.c. circuit may be made small. The arrangement also has obvious disadvantages and is little used.

(b) Parallel feed

The " parallel (or shunt) feed " circuit is shown in Fig. 27.32. In this arrangement a blocking capacitor is necessary to prevent a low resistance d.c. path being formed from grid to earth by the tuning inductor. The resistors R_8, R_9 and R_{10} provide part of the d.c. path from the valve grids back to the cathodes. Since the individual resistors are shunted across their corresponding tuned circuits, the values selected must not be too low as otherwise appreciable damping occurs. A 0.5 megohm resistance in parallel with a typical r-f tuned circuit generally is not serious, but could appreciably reduce the dynamic resistance of an i-f circuit. For these reasons " parallel feed " is sometimes used with r-f stages, but it is seldom applied to i-f stages, and receivers are often designed to use both systems of a.v.c. feed.

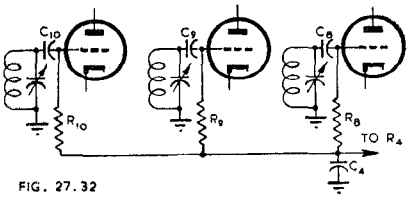


FIG. 27.32

" Parallel feed " for the r-f stages is sometimes more convenient than " series feed," and appears to be satisfactory in most respects, although it has been found that grid blocking is more likely to occur with " parallel feed " than with " series feed."

With any method of feed it is important that the total resistance in the grid circuit should not exceed the maximum for which the valves are rated. Depending on the characteristics of the particular valve type and the effects on electrode dissipations and total cathode current, as determined by equation (6) on page 82, the following maximum values of grid resistor may be used as a general guide.

For one controlled stage	3 megohms
For two controlled stages	2.5 megohms
For three controlled stages	2 megohms

These resistances are to be measured between the grid of any valve and its cathode.

The values above assume that the receiver is normally tuned to a station and that the controlled valve or valves are operating at reduced cathode currents and transconductance, as determined by the a.v.c. bias.

(v) Typical circuits

A typical circuit of a simple a.v.c. system, with three controlled stages, is shown in Fig. 27.33. In order to provide the simplest arrangement the cathode of the duo-diode valve is earthed and grid bias is obtained for the triode section by the grid leak method using a resistor of 10 megohms. This method of biasing reduces the a.c. shunting across the diode load resistor. The cathodes of the controlled stages are normally returned to a point of positive voltage to ensure that the recommended negative grid bias is obtained for conditions where the input signal is very small ; cathode bias is the usual arrangement.

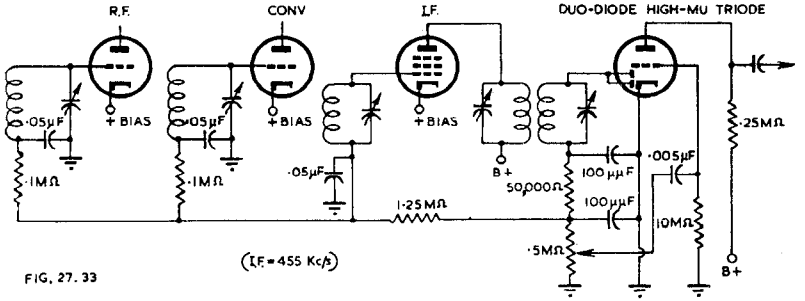


FIG. 27.33

The circuit values shown are typical for an intermediate frequency of 455 Kc/s. An a.v.c. resistor of 1.25 megohms is used so that the total resistance to earth from any grid does not exceed 2 megohms. If there were only two controlled stages this could be increased to about 1.75 megohms with a consequent decrease in the a.c. shunting.

A typical delayed a.v.c. circuit is shown in Figs. 27.34. Cathode biasing is used for the pentode section of the duo-diode pentode valve, and since the bias will usually be about two or three volts this also provides a suitable a.v.c. delay voltage without any further complication. With circuits using delay voltages on the a.v.c. diode the bias due to automatic volume control on the controlled valves is zero until the peak voltage on the diode exceeds the delay voltage. The controlled stages are arranged to have a self-bias voltage equal to the recommended minimum grid-bias voltage.

(vi) A.V.C. application

Automatic volume control is normally applied to the converter on the A-M broadcast band, irrespective of valve type. On the short-wave band some types of converters give very satisfactory operation with an a.v.c. bias voltage applied to the signal grid, while others introduce difficulties because of the appreciable shift in oscillator frequency caused by the changing signal grid bias. When no r-f stage is used it is often necessary to apply a.v.c. to the converter, but when a r-f stage is incorporated

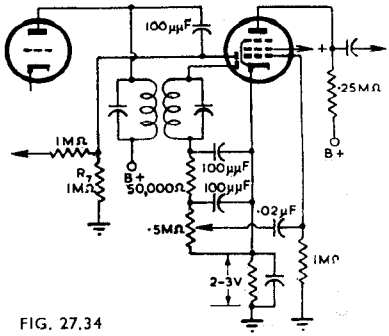


FIG. 27.34

it is frequently advantageous to operate valve types 1A7-GT, 1C7-G, 6A8, 6D8-G on fixed bias. Valve types 6J8-G, 6K8, 6BE6, 6SA7 and all triode hexodes may be used with a.v.c. on A-M broadcast and short wave bands*. For receivers operating in the 88-108 Mc/s F-M broadcast band, a.v.c. bias is not applied to the signal grid of the converter valve ; very often on this band fixed bias is used for the r-f stage, and a.v.c. is applied to the i-f stages only. Whether a.v.c. is used at all with these receivers often depends largely on the type of detector, but it is advisable to avoid overloading of the early stages so as to reduce the possibility of the generation of undesired spurious responses ; this often calls for a.v.c. bias to be applied to the r-f stage.

Some oscillator frequency shift occurs with all types of converters when the signal grid bias is altered. With valve types such as the 6A8 operating on the short wave band the reception of a fading signal is difficult since the variations caused by a.v.c. bias may cause the signal to swing in and out of the pass band of the receiver. An even greater difficulty occurs when the receiver is being tuned to a strong signal, since the magnitude of the output will be different when tuning in from either the high frequency or the low frequency side of the signal. Very careful adjustment is required to obtain the best tuning position. A rather similar effect has been noticed on both the broadcast and short-wave bands, but in this case the effect is generally due to faulty gang wipers. When this is the cause it can occur with any type of receiver (t.r.f. or superheterodyne), but with superheterodynes the oscillator section of the ganged capacitor should be checked first, as this is generally the one causing most of the difficulty.

With ordinary broadcast receivers having a r-f stage, converter, and a single i-f stage, automatic volume control is normally applied to all three stages. If decreased modulation rise is required it is preferable to operate the i-f stage with about one-half of the full a.v.c. bias or, alternatively, to supply the screen voltage by means of a series resistor ; the latter arrangement is the more usual one in practice. Negligible modulation rise is possible, with effective a.v.c. action, if all control is omitted from the i-f stage, but difficulties such as those due to decreased signal-to-noise ratio must not to be overlooked when this system of a.v.c. is used on a number of tuning ranges (see (iii) above).

In a receiver without a r-f stage it is difficult to avoid overloading with large input signals, and a.v.c. is applied to both stages even though modulation rise may be objectionable with very high inputs. In order to obtain maximum control the screen voltage for the i-f valve should be obtained from a voltage divider. The degree of control must, however, be weighed against the possibility of non-linear distortion ; this factor has already been discussed in Chapter 26 in connection with distortion in i-f amplifiers.

For a receiver having two i-f stages the second stage should preferably be operated at fixed bias in order to prevent modulation rise. It is possible that better overall performance at high input signal levels will be obtained when the second i-f stage is operated at a negative bias somewhat greater than the minimum bias. Removal of control from the last i-f valve will often reduce the possibility of overloading this stage, although this is not always a good solution as will be discussed in (xv) below.

(vii) Amplified a.v.c.

There are a number of methods available whereby the a.v.c. voltage to be applied to the controlled stages can be amplified, either before or after rectification.

(a) One or more stages of amplification may be used to form an a.v.c. amplifier channel operating in parallel with the signal channel, and having a separate diode rectifier. If the total gain of the a.v.c. amplifier channel is greater than the total gain of the equivalent section of the signal channel, there is effectively a system of amplified a.v.c. This is more effective than the usual arrangement with a single channel, since it retains the full amplification of the a.v.c. channel under all conditions. It also has advantages in flexibility due to the isolation of the two channels, and the a.v.c. channel may be designed to have any desired selectivity characteristics.

*See also Chapter 25 Sect. 2 pages 990-1001.

(b) If a common i-f channel is used, it is possible to add a further i-f stage with fixed bias for a.v.c. only, followed by a separate a.v.c. rectifier. By this means it is possible to avoid the distortion due to shunting of the diode load resistor, or to " differential loading " at a point where the a.v.c. delay is just being overcome.

(c) A d.c. amplifier may be used to amplify the voltages developed at the rectifier. A typical circuit arrangement giving d.c. amplified a.v.c. is shown in Fig. 27.35. Design methods are given in Refs. 44 and 45.

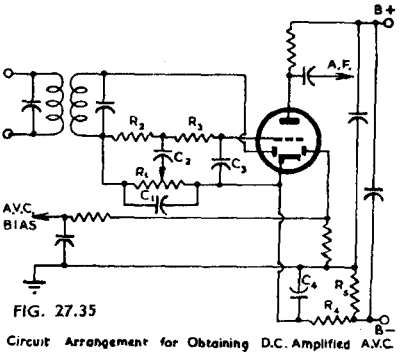


FIG. 27.35
Circuit Arrangement for Obtaining D.C. Amplified A.V.C.

See also Fig. 27.43 and the description given in Sect. 4(ii) later in this chapter.

(viii) Audio a.v.c.

Audio a.v.c. is sometimes used in radio receivers in conjunction with a.v.c. applied to the r-f and i-f stages to flatten out the overall a.v.c. characteristic. Whole or part of the a.v.c. bias voltage is applied to an audio frequency voltage amplifier valve having a grid with a variable-mu characteristic.

It should be clear that conventional a.v.c. systems cannot give a perfectly constant a-f output with a varying input voltage, because conventional a.v.c. is a " back-acting " device in which the effect on the controlled stages must follow the change occurring at a later stage in the receiver. Audio a.v.c. is " forward-acting " and so a constant or even a drooping characteristic is possible for increasing signal input voltages. Simple audio a.v.c. systems tend to introduce a considerable amount of non-linear distortion into the audio output voltage when the signal input voltage is large. This is due to the curvature of the $g_m - e_g$ characteristic of the controlled valve.

The amount of distortion can be reduced to negligible proportions by the use of elaborate circuits, but as these systems generally require an additional a-f amplifier valve they are not used to any extent in commercial radio receivers.

If it is decided that audio a.v.c. is desirable, the usual procedure is to obtain the best possible a.v.c. characteristic, apart from the a-f amplifier, and then to add just

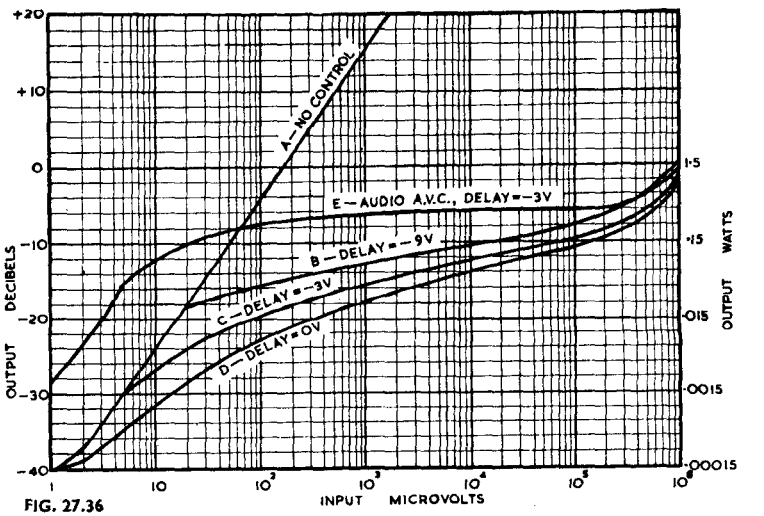


FIG. 27.36

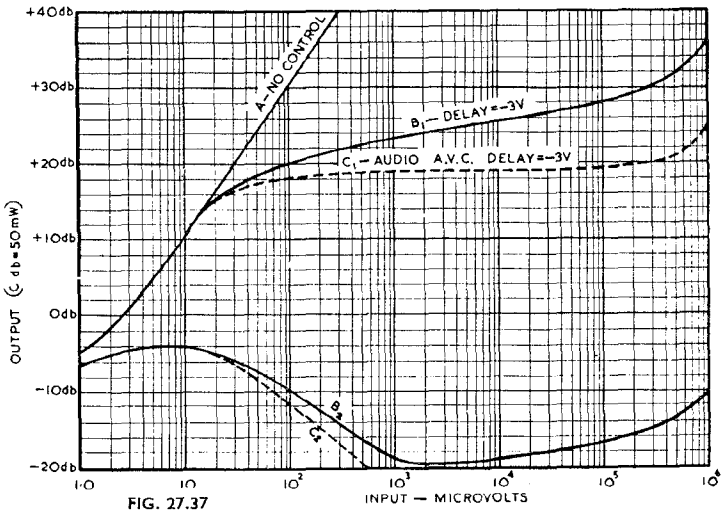


FIG. 27.37

enough a.v.c. bias voltage to the a-f amplifier to give the required overall results. The improvement in the overall a.v.c. characteristics, when audio a.v.c. is used, can be seen from Figs. 27.36 and 27.37.

An example of combined a.v.c. occurs in receivers using a reflexed voltage amplifier stage (see Chapter 28). In this case the a.v.c. bias voltage applied to the valve control grid is effective in controlling both the i-f and a-f gain, and if properly used the system can be made to assist very materially in obtaining good a.v.c. characteristics from a receiver having only one other controlled stage, namely the converter stage in the usual receiver. Another example of a circuit using audio a.v.c. is shown in Fig. 27.45.

(ix) Modulation rise

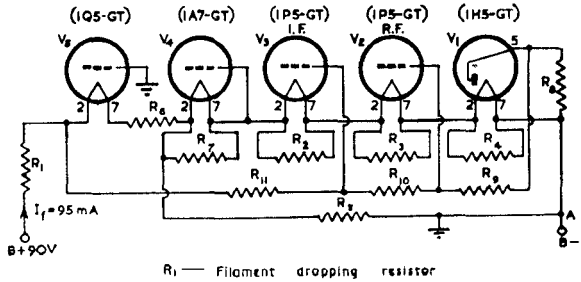
When a modulated carrier voltage is applied to a voltage amplifier stage in which the valve has a curved $g_m - e_g$ characteristic, the modulation percentage will increase. This modulation rise is noted in the output as audio frequency harmonic distortion (non-linear distortion), mainly second harmonic. Practically all of the modulation rise occurs in the final i-f stage. 20% modulation rise is equivalent approximately to 5% second harmonic. Modulation rise with fixed bias is extremely small even with remote cut-off valves, but there is a slight advantage in using a valve having a sharp cut-off characteristic. Modulation rise may be decreased by operating the i-f stage on a fraction of the a.v.c. voltage, but this adds to the expense of the receiver. Alternatively, a noticeable improvement may be made by supplying the screen from a series dropping resistor connected to B+. This is recommended for circuits having one r-f and one i-f stage. Modulation rise can sometimes be reduced by increasing the gain from the grid of the final i-f valve to the a.v.c. diode. Improving the amount of control on the earlier stages by reducing the screen voltage (this provides cut-off with lower grid voltages) will help in reducing modulation rise, but is likely to lead to difficulties with cross modulation when the receiver is used in close proximity to a powerful transmitter.

(x) A.V.C. with battery valves

When battery valves operating at zero bias are used, it is possible to obtain delayed a.v.c. by incorporating a duo-diode-triode or duo-diode-pentode valve having a diode plate situated at each end of the filament. A delay of between 1 and 2 volts (depending on the filament voltage) is obtainable by this means, and makes a very simple and satisfactory arrangement. The diode at the positive end of the filament is used for

a.v.c. and its return is taken to filament negative. The diode at the negative end of the filament is used for detection and its return is taken to filament positive.

It sometimes happens that the filaments of battery valves are operated in series or series-parallel arrangements. Under these conditions it becomes more difficult to design an efficient a.v.c. system than when parallel filament operation is used. In the usual type of a.v.c. circuit the grid returns from the several controlled stages are brought to a common point, and the zero signal grid voltage on these stages is the same. With series or series-parallel operation, however, the filament voltages differ with the result that the zero signal bias on one or more stages may differ from zero by a multiple of the filament voltage. Circuit arrangements which allow the bias on the grids to be zero for no signal input generally allow only a reduced proportion of the a.v.c. voltage developed by the diode to be applied to some of the controlled stages; full a.v.c. bias can only be applied to one or two stages in most cases. Fig. 27.38A shows a typical circuit arrangement for the case where the filaments are connected in series and operated from the H.T. supply. The a.v.c. voltage divider is made up from the resistors R_8, R_9, R_{10} and R_{11}. A value of about 2 megohms is usual for R_{10} while R_{11} is made about 2 megohms per 1.3 volt drop, in the case of 1.4 volt valves (which are operated with 1.3 volts as a recommended value for the series filament connection). In the circuit shown a higher proportion of the a.v.c. control voltage is applied to valve V_2 than to valve V_3. The purpose of the resistors R_7, R_2, R_3, R_4 and R_5 is to allow the correct filament voltage to be applied to each of the valves, since it should be obvious that the valve V_1, at the negative end of the chain, carries the total cathode current for all the valves, and each of the other valves carries the cathode currents for all the other valves which are nearer to the positive end of the chain than the valve being considered. This statement is modified when R_5 is used, because this provides an alternative path for the cathode currents. From this it follows that no shunting resistor is required for V_5



R_1 — Filament dropping resistor

R_2, R_3, R_4, R_7 — "Cathode current" shunting resistors

R_5 — Filament current shunting resistor

R_6 — Bias resistor

R_8 — Diode load

R_9 — A.V.C. filter resistor

R_{11}, R_{10} — A.V.C. grid bias" resistor

FIG. 27.38A

(xi) Special case with simple a.v.c.

If a simple a.v.c. circuit, such as that shown in Fig. 27.28, is used in conjunction with a diode-pentode (or triode) operating with cathode bias, the diode load return will be two or three volts above earth. It is necessary, in this case, to provide additional negative bias voltage on the controlled stages if the correct minimum bias voltage is to appear between grid and cathode in each case.

(xii) The a.v.c. filter and its time constants

There are several reasons why filter circuits, such as those shown in Fig. 27.33, are required. One important reason is to prevent r-f and a-f voltages which appear

across the a.v.c. diode load from being applied back to the grids of the controlled stages. If r-f or i-f voltages are applied back to the grids then instability troubles are certain to arise. A-F applied to the grids can lead to a reduction in the percentage of modulation present on the carrier. Inter-stage filtering is also necessary because undesired coupling can lead to instability and spurious whistle responses. From this it can be seen that the prime function of the filter circuits is to allow only the d.c. voltage developed across the diode load to be applied as additional bias on the controlled valves. The components making up the filter also serve the necessary function of completing the r-f and i-f circuits through low impedance paths and, furthermore, the resistors serve to complete the d.c. return path between grid and cathode of each controlled valve so that the correct negative bias voltage can be applied.

It is not permissible to choose values of resistance and capacitance at random if satisfactory circuit operation is to be obtained. Several conflicting factors must be considered when the component values are being selected. The time constant (defined below) of the filter network, must be low enough so that the a.v.c. bias voltage can follow the changes in signal input voltage with sufficient rapidity to offset the effects of fading. Limiting values for the total circuit resistance have been stated in (iv) above, and the choice of suitable values for R and C will be discussed as we proceed, but first the expression " time constant " will be defined.

The " time constant " of a resistance-capacitance network is the time in seconds required for the capacitor to acquire sufficient charge for the voltage between its plates to be equal to 63.2% of the total voltage applied to the circuit. Alternatively, it is the time taken for a charged capacitor to lose sufficient charge for the voltage across its plates to fall to 36.8% of the initial voltage existing between the plates in the fully charged condition. It is a simple matter to show that, for the conditions stated, the time constant (T) is given by

$$T = RC \text{ seconds}$$

where R = circuit resistance in ohms
and C = circuit capacitance in farads.

(It is usually more convenient to write

T = resistance in megohms × capacitance in microfarads = seconds).

If the total resistance in the circuit is altered in any way from its value during the charging operation to a different value during the discharge of the capacitor, then it is helpful to use the terms " charge time constant " and " discharge time constant." In a.v.c. circuits there is always a difference between the charge and discharge time constants, because during charge the diode is conducting and its conduction resistance effectively short-circuits the d.c. diode load resistor. This also means that the " charge time constant " is always more rapid than the " discharge time constant " in these circuits.

Suitable values for " charge time constants " are

Broadcast good fidelity receivers	0.25 to 0.5 second
Broadcast receivers	0.1 to 0.3 second
Dual wave or multi-band receivers	0.1 to 0.2 second

For the reception of telegraphy longer time constants are often required to ensure silence between signals, and a value of about 1 second is often used. In any good quality communications receiver it is usual to provide facilities for selecting any one of a number of a.v.c. time constants. This enables the operator to select the most suitable condition to offset the particular type of fading being encountered. Too rapid a time constant is not selected for high quality broadcast reception as rapid fading would cause bass-frequency anti-modulation and so reduce the audio frequency bass response. See also Chapter 35 Sect. 3(i)B2, page 1233.

In broadcast receivers the charge and discharge time constants are often very nearly equal. However, for some types of reception it may be preferable for the charge time constant to be rapid to prevent the beginning of a signal from being unduly loud, but the discharge time constant is made comparatively slow to prevent a rapid rise in noise output during intervals between signals (see also Ref. 43, p. 181).

The procedure for calculating charge and discharge time constants is as follows. Consider Fig. 27.30 in conjunction with Fig. 27.28, then

For 2 stages

Charge time constant =

$$R_1(C_2 + C_4 + C_5) + R_4(C_4 + C_5) + R_5C_5$$

Discharge time constant =

$$C_5(R_5 + R_4 + R_2) + C_4(R_4 + R_2) + C_1(R_1 + R_2) + C_2R_2.$$

These follow readily when it is considered that the diode is conducting during charge, and $R_1 \ll R_2$; the diode is non-conducting during discharge.

For 3 stages

Charge time constant =

$$R_1(C_2 + C_4 + C_5 + C_6) + R_4(C_4 + C_5 + C_6) + R_5C_5 + R_6C_6.$$

Discharge time constant =

$$C_6(R_6 + R_4 + R_2) + C_5(R_5 + R_4 + R_2) + C_4(R_4 + R_2) + C_1(R_1 + R_2) + C_2R_2.$$

If the circuit of Fig. 27.28 were considered alone the charge time constant would be $R_1(C_2 + C_4) + R_4C_4$ (assuming $R_2 \gg R_1$), and the discharge time constant $C_1(R_1 + R_2) + C_2R_2 + C_4(R_4 + R_2)$. The way in which the total time constant is built up for the more complicated cases will be readily seen, and the addition of extra controlled stages should offer little difficulty when the new time constants are to be determined.

For a more detailed discussion of time constants in a.v.c. circuits the reader is referred particularly to Ref. 47.

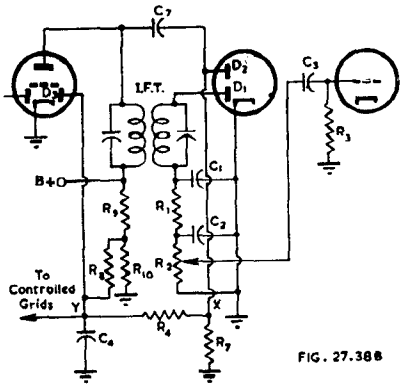


FIG. 27.38B

Fig. 27.38B. Circuit for "sinking diode" arrangement which reduces differential distortion.

(xiii) A.V.C. characteristics

A.V.C. Characteristic Curves may be plotted on 6 cycle log-linear graph paper as shown in Fig. 27.36. The input is usually taken from 1 μV to 1 volt. The output is usually shown in decibels, with an arbitrary zero reference level. The complete curves are useful not only for demonstrating the effectiveness of the a.v.c., but also to indicate modulation rise.

To facilitate the developmental work on the complete receiver it is helpful to draw on the same graph

(a) A curve of distortion against input voltage for 30% modulation at 400 c/s.
(b) A curve of the developed a.v.c. voltage against input voltage.
(c) Curves of the total bias voltages on the controlled stages against input voltage.
(d) A curve of noise output against signal input voltage*. This allows the signal-to-noise ratio, for any input voltage to be determined.

If fixed minimum bias is used, curves (b) and (c) will differ only by the bias voltage. If self-bias is used they will differ by the minimum bias voltage present with no input voltage, and will tend to run together at high input voltages. For methods of conducting the experimental measurements see Chapter 37.

*See also Chapter 35 Sect. 3(i) pages 1229-1234.

Fig. 27.36 shows several a.v.c. curves, each corresponding to a particular condition. In taking these curves two separate diodes were used to maintain constant transformer loading and other conditions. Contact potential in the diode results in a slight increase in the standing bias voltage on the controlled stages ; this effect has been discussed in (ii) above.

Curve A is the " no control " characteristic and is the curve which would be followed, with the a.v.c. removed from the receiver, up to the point at which overloading commences. This characteristic is a straight line and the slope is such that an increase of ten times in the input voltage gives a 20 db increase in output.

Curve B is the a.v.c. characteristic for a delay of −9 volts. For inputs of 3 to 18 μV the experimental curve follows the no control line exactly, and then deviates sharply for inputs above 18 μV. From 18 to 500 000 μV the slope of the curve is fairly constant, the output increasing by about 3.25 db for each 10 times increase in the input voltage. Above 500 000 μV (i.e. 0.5 V) input the curve tends sharply upward, indicating severe modulation rise.

Curve C is the a.v.c. characteristic for a delay of −3 volts. The a.v.c. comes into operation at a lower input voltage, as would be expected, and the average slope is steeper than for the higher delay voltage. In both cases, however, the " knee " of the curve as it leaves the no control line is very clearly defined.

Curve D is the a.v.c. characteristic for a delay of zero voltage, with due compensation for the effect of contact potential on the standing bias of the controlled valves.

Curve E is typical of the characteristics obtained when audio a.v.c. is added to a receiver. Over the range of inputs from 100 to 500 000 μV the total rise in output is only 3 db.

Curve B has been drawn according to the conventional method whereby the output is adjusted to half the maximum undistorted output of the receiver for an input signal of 1 volt. Curves C and D were then taken directly, without any further adjustment to the volume control. Owing to a slight effect on the gain of the receiver when the delay voltage is varied, Curves C and D fall slightly below the datum line at an input of 1 volt. Curve E has been drawn to correspond to Curve C, since both have the same delay voltage. The volume control, however, was advanced considerably for Curve E. It should be noted that no conclusions should be drawn from the relative vertical positions of a.v.c. characteristics drawn according to the conventional method since the volume control settings are unknown.

(xiv) An improved form of a.v.c. characteristic

The conventional method of obtaining a.v.c. characteristics does not give all the information which is available, and an improved method yielding additional data has been suggested by M. G. Scroggie (see Ref. 51). This method will now be described.

Instead of commencing at an input of 1 volt and adjusting the volume control to give one-quarter or one-half of the maximum undistorted power output at 30% modulation, Scroggie's method is to commence at a low input voltage with the volume control set at maximum. The input is increased until the output is approximately one-quarter of maximum, and the volume control is then set back to reduce the power output to one-tenth of the reading. This process is repeated until an input of 1 volt (or whatever is the maximum available from the signal generator if this is less than 1 volt) is reached.

This method is illustrated by the curves shown in Fig. 27.37. The scale of power output represents the output (at 400 c/s) which would be obtained with the volume control at maximum and 30% modulation, provided that no overloading occurred in the audio amplifier. A number of interesting facts may be obtained from an examination of these curves.

1. The residual noise level of the receiver may be shown.
2. The sensitivity of the receiver in microvolts input for any selected output level (e.g. 50 mW or 0.5 W) may be read directly from the curves. It should be noted that the output includes noise.

3. The power output corresponding to any selected input voltage and any position of the volume control may be obtained. For example, with a delay of −3 volts (curve B1) the delay voltage is overcome at an output level of slightly less than 2 watts with the volume control set at maximum. As a further example (again assuming 400 c/s and 30% modulation) take the same curve at an input of 1000 μV, where the output is shown as approximately 10 watts with the volume control at maximum. The setting of the volume control to give 4 watts output and using 100% modulation instead of 30% is

$$\sqrt{(30/100)^2 \times (4/10)} = 0.11$$

of the maximum resistance of the control. The actual amount of rotation will depend on whether the volume control resistance is related to rotation by a linear or a logarithmic law.

4. The voltage at the detector may be calculated from a knowledge of the a-f gain and the detection efficiency. The a.v.c. bias voltage can also be determined indirectly by calculation from the data obtained.

5. The slope of the initial part of the curve can show up an under-biased valve in the receiver. Cheap receivers frequently use a common source of bias for two or more valves, and under these conditions it can happen that one of the valves has too little bias and gives less than its maximum gain when there is no signal input to the receiver. As the input is increased, a.v.c. is applied to each controlled valve and this gives a comparatively rapid increase in gain from the under-biased valve. Such an increase shows up as an early section of the a.v.c. curve with a slope more vertical than it would otherwise be—usually with a slope in excess of 6 db per octave—and with a noticeable bend towards the horizontal at the point at which the valve receives the bias required for maximum sensitivity.

To operate a valve under these conditions is of course undesirable, and in use the receiver will emphasize the fading of any signals which fade through the range of signal inputs over which the effect operates.

6. The signal-to-noise ratio for any input can be read directly from the graph, as mentioned previously. In addition, the increments of signal-to-noise ratio with increasing input can be checked. An ideal receiver would give a 20 db improvement of signal-to-noise ratio for each 20 db increase in input, and it is possible for a normal receiver to approach this value, at least over the first decades of the a.v.c. graph. Any significant departure from the ideal can usually be traced to the application of a.v.c. to the first valve in the receiver [see Chapter 35 Sect. 3(i)] and care should be taken to keep the signal-to-noise ratio improving as rapidly as possible until it has reached a value of at least 45 db.

Scroggie's method makes possible the measurement of ratios as great as this, or much greater, because although one reading, the power output, may be beyond the range of the output meter used, the volume control of the receiver is in effect used as a multiplier.

7. The noise curve of the receiver might be expected to decrease indefinitely with increasing a.v.c. voltage, but there are two reasons why it may not do so. The first is that although the object of the test is to measure the signal-to-noise ratio of the receiver, in practice the signal-to-noise ratio of both the signal generator and the receiver are being measured. A 50 db ratio between 30% modulation and residual noise with no modulation is a representative figure for a signal generator of reasonable quality, and it is generator noise which causes the noise curve in Fig. 27.37 to become approximately horizontal shortly after 1000 μV input.

The second reason for the noise curve not decreasing indefinitely is that in most receivers in which power supply filtering has been kept to a minimum, for reasons of economy, there is some modulation hum with high inputs. This hum shows up as an increase in the level of the noise curve, and by plotting the curve over the full range of inputs expected to be applied to the receiver the designer can assure himself that the level of modulation hum does not become objectionable. An increase in modulation hum can be seen in Fig. 27.37 as the input approaches 1 volt.

The a.v.c. characteristics in Fig. 27.37 can be taken as typical of curves taken by this method. B_1 and B_2 show the signal and noise curves respectively for a 5 valve receiver without audio a.v.c. and C_1 and C_2 show the results for the same receiver with audio a.v.c. It will be seen that the delay is overcome at about 15 μV input and that at say 0.1 volt input there is $8\frac{1}{2}$ db of audio control by the a.v.c. The noise ratio ($B_1 - B_2$) should be identical with the ratio ($C_1 - C_2$) since the only difference between the B curve and the C curves is that due to modified audio gain. Thus the curve C_2 would become approximately horizontal at 2000 μV input and at -25 db.

This method enables greater accuracy to be obtained for very small input signals since the power output reading will be well up on the scale of a typical output meter. With the conventional method the output is too small to measure accurately with a standard type of output meter.

At extremely low input voltage levels the noise fluctuations make accurate output measurements very difficult to carry out.

(xv) Design methods

One of the difficulties faced by a receiver designer in making a preliminary calculation of the a.v.c. performance of a receiver is often the lack of complete data on some of the valve types he is expected to use. If a completely satisfactory preliminary design is to be made it is necessary to have available, firstly, data on the manner in which mutual or conversion conductance varies with grid bias voltage ; this data must be for conditions of fixed screen voltage, and also for the case where the screen voltage is applied by means of a series dropping resistor. The second requirement is to know for a given percentage of non-linear distortion the signal handling capabilities (input and output) for various grid bias voltages, of the valves to be used in the controlled stages ; this knowledge is required particularly in the case of the last (and sometimes an earlier stage, as will be discussed below) i-f voltage amplifier valve when a large delay bias is used on the a.v.c. diode. Diode characteristics are also required, but these are usually available. The requirements of valve data are partly fulfilled in some cases, and for later valve types some additional information is available.

Because of the time required to carry out measurements to obtain the additional data, receiver designers, in the majority of cases, make only a few preliminary calculations to determine the desired time constants etc., and then proceed to achieve suitable a.v.c. characteristics by experimental procedures. As an example, with broadcast receivers it is usual to take the cathode bias voltage used for control grid bias on the multi-element valve containing the a.v.c. diode as providing sufficient a.v.c. delay bias (this bias is generally about -3 volts) and with the usual series of valves (e.g. 6SK7, 6J8-G etc.) and transformers a reasonably satisfactory a.v.c. characteristic is obtained ; this assumes that component values are used which are of the order of those discussed in previous sections in connection with Figs. 27.33, 27.34 etc. For the type of receiver where improved a.v.c. characteristics are called for, a fairly large delay bias may be used on the diode. In general, the higher the delay voltage the flatter will be the a.v.c. characteristic (over the range of a.v.c. operation) and this is illustrated by Fig. 27.36. The limitation on the allowable amount of delay bias is set, however, by the magnitude of the signal voltage appearing at the grid and plate of the last i-f amplifier valve, and it is for this reason that, when large delay bias voltage is used, the i-f valve is sometimes operated with reduced or zero a.v.c. bias. However, as this reduces the number of controlled stages it is not necessarily a satisfactory solution, and a better arrangement is to use an additional stage to obtain the necessary control.

Design examples

Attention will be confined mainly to simple delayed a.v.c. systems of the more common types. For additional design information and discussion the reader is referred to Refs. 45, 44, 43 and 53. A good practical approach to the problem is given in Ref. 43.

(1) A receiver is to have one r-f and two i-f stages controlled by a.v.c. ; the converter operates with fixed bias. It is required to estimate, roughly, the diode delay

bias required if the detector output voltage is not to change by more than 6 db for a change in signal input to the aerial stage of 50 db.

Assume first that the a.v.c. and signal detectors are linear, that equal signal voltages are applied to the detector and a.v.c. diodes, and that the detection efficiency (η) is unity. Since stage gain varies with change in mutual conductance (g_m) it can be taken, with typical voltage amplifier valves, that the gain alters by about 1.5 db for each additional volt of negative grid bias (this can be determined with greater accuracy from similar methods to those given later). Since there are three controlled stages using similar valves, the total gain decrease is 4.5 db per volt of bias. (Suppose similar valves are not used, one valve giving a gain change of 2 db per volt of bias and two others giving 1.5 db per volt, then obviously 1 volt of a.v.c. bias change alters the receiver gain by 5 db).

The total decrease in receiver gain which is required equals 50-6 = 44 db. To achieve this the additional a.v.c. bias needed is 44/4.5 = 9.8 volts. That this is also equal to the delay bias required for the stated conditions, can be appreciated because, at the threshold of a.v.c. operation, the voltage on the detector diode will be 9.8 volts peak, and for a further 9.8 volts (peak) increase in signal input the total voltage applied to the detector is 19.6 volts giving an increase in a-f output voltage of 6 db. The effect of 19.6 volts (peak) signal applied to the a.v.c. diode is to produce the required 9.8 volts d.c. bias since half the peak input voltage is required to overcome the delay voltage.

To illustrate a further point, suppose it had been taken that an 80 db input change should only give 6 db output voltage change. Then the delay bias required would be (80-6)/4.5 = 16.4 volts. This also means that the stage preceding the detector must deliver 32.8 volts peak when the carrier is constant. During modulation of the carrier the peak voltage delivered by the last i-f stage can reach 65.6 volts, and if distortion is to be avoided the valve preceding the detector must be capable of delivering this amount of output voltage when the total bias is 16.4 volts plus the standing bias. Whether this is possible can be determined from curves of the signal handling capability of the valve in question, or by direct measurements using a modulated carrier. It will be found, usually, that the maximum output voltage which can be handled without severe distortion is very much reduced when the grid bias voltage is large. This then suggests that reducing the a.v.c. bias on the last i-f amplifier valve will allow the permissible plate voltage swing to be increased. Reducing the bias voltage also results in the stage gain being increased, and so the same a.v.c. bias voltage is produced with a smaller signal input voltage. However, the amount of total control is reduced, and so partial or zero a.v.c. bias on the last i-f valve is not necessarily a satisfactory solution in every case.

It should be observed that the last i-f stage is not necessarily the one in which overloading will occur first. In Chapter 26, when discussing the crystal filter stage, it was pointed out that the grid to plate gain of the valve preceding the filter was very high with the arrangement shown. Suppose the grid to plate gain of the first valve is 400 times, but the gain from the grid of the first to the grid of the second valve (into which the filter feeds) is 5 times, then if the grid to plate gain of the second valve is less than 80 times it becomes immediately apparent that the first i-f valve will be overloaded before the second one. Extreme cases of this type are not likely to occur, but they present possibilities which should not be overlooked.

(2) A detailed design for a single controlled stage is to be carried out from valve data. Simple a.v.c. is to be used.

The valve type selected for this example is the 6SK7 remote cut-off pentode. The average characteristics are shown in Fig. 27.39. The standing bias is −3 volts and the mutual conductance (g_m) for this condition is 2000 micromhos. For a total grid bias of −35 volts the g_m is 10 micromhos. If cathode bias were used some additional error would be introduced, although this is usually neglected.

The first step is to convert the $g_m - E_g$ curve of Fig. 27.39 to a curve showing the change in gain of the controlled stage with variation in grid bias. The actual value of stage gain is not required since it is assumed to be directly proportional to g_m.

The change in g_m is expressed in decibels, taking as the reference level (0 db) the value of g_m for maximum gain, i.e. the g_m with only the standing bias (−3 V) applied to the grid. In this case the g_m used for zero reference level is 2000 micromhos. Then using

$$\text{Change in gain (db)} = -20 \log_{10} \frac{g_m(E_{c1} = -3\text{ V})}{g_m} = -20 \log_{10} \frac{2000}{g_m}$$

the following values are obtained (the values for g_m are taken from Fig. 27.39).

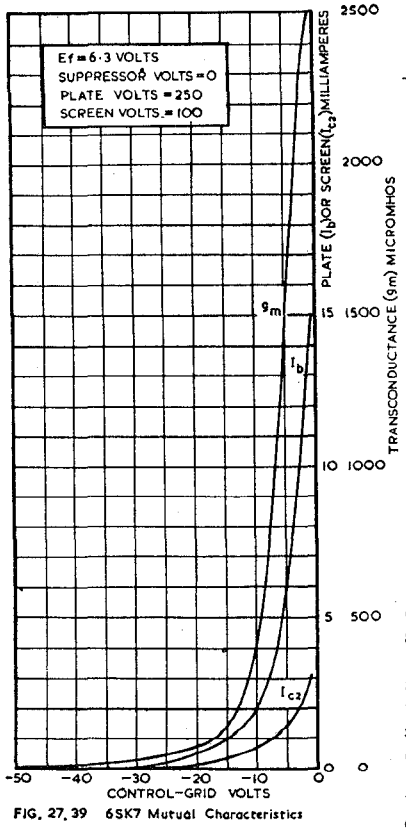


FIG. 27.39 6SK7 Mutual Characteristics

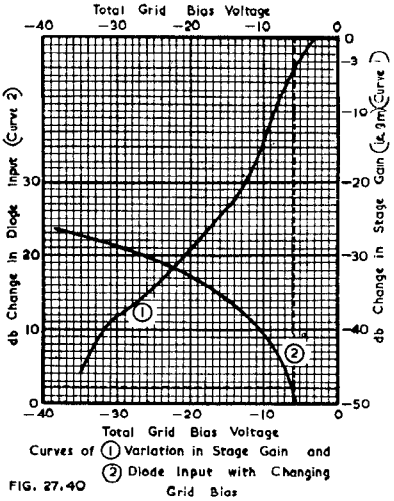
Total Grid Bias*	g_m	Change in Gain (db)
−3	2000	0
−4	1750	− 1.15
−5	1438	− 2.86
−6	1200	− 4.44
−7	925	− 6.69
−8	700	− 9.13
−9	520	−11.7
−10	383	−14.4
−12.5	225	−19
−15	138	−23.2
−17.5	90	−26.9
−20	70	−29.1
−22.5	50	−32
−25	40	−34
−27.5	30	−36.5
−30	25	−38
−32.5	18	−41
−35	10	−46

*= − (3 + a.v.c. bias).

These results are plotted in Fig. 27.40 as curve 1. It might be noted that the average slope is 1.4 to 1.5 db per volt.

It is next required to determine the amount of a.v.c. bias voltage developed by the diode circuit, for various input voltages applied to the diode. In a typical case the d.c. diode load resistance would be 1 megohm, and the d.c. voltage developed for various signal input voltages can be taken directly from Fig. 27.6. The developed d.c. voltages are tabulated in column (2) below against r.m.s. signal (E_{rms}) applied to the diode.

E_{rms} (= signal input to diode)	A.V.C. Bias (volts)	Total bias (= A.V.C. + standing bias)	Diode Signal Input Change (db)
2	− 2.2	− 5.2	0
5	− 6.2	− 9.2	8
8	− 9.1	−12.1	12
10	−11.8	−14.8	14
15	−17.8	−20.8	17.5
20	−23.9	−26.9	20
30	−35.6	−38.6	23.5



Curves of ① Variation in Stage Gain and ② Diode Input with Changing Grid Bias

FIG. 27.40

It is now necessary to relate the total bias (a.v.c. + standing bias) to the **change** in diode input voltage ; the change is conveniently expressed in decibels. Any signal voltage applied to the diode may be taken as zero reference level (0 db), and in our case $E_{rms} = 2$ volts will be convenient. Then the change in diode input voltage is given by,

$$\text{db change in diode input} = 20 \log_{10} \frac{E_{rms}}{E_{rms}\ (\text{for total bias} = -5.2\ \text{V})}$$

$$= 20 \log_{10} \frac{E_{rms}}{2}$$

The results are tabulated in column (4) of the table given above, and the total bias versus diode signal input change is plotted as curve (2) in Fig. 27.40.

Finally, it is required to find the way in which the output changes with changes in signal input to the amplifier. If we assume various values for the change in signal voltage applied to the diode, it is a simple matter to determine the total grid bias, and from this the change in stage gain, by using curves (2) and (1) Fig. 27.40. Also from the curves, it is seen that, with zero change in diode input (0 db), the amplifier stage gain is 3 db down on the maximum possible gain. (This is because we selected $E_{rms} = 2$ volts as being the zero reference level). If now we assume, say, 2 db change in diode input, the actual change in stage gain is $-4.3 - (-3) = -1.3$ db. Because voltage input applied to the diode has increased 2 db, and the amplifier stage gain has decreased 1.3 db, it follows that the signal voltage applied to the amplifier grid must have increased $2 + 1.3 = 3.3$ db.

The direct output voltage change across the detector load, for 3.3 db change in signal input, is from -2.2 volts to -2.9 (i.e. from curve (1), Fig. 27.40, the total bias voltage change is from -5.2 to -5.9 volts, which correspond respectively to -2.2 volts and -2.9 volts across the diode load, when the standing bias is -3 volts). Expressing the direct output voltage change in decibels, we have

$$\text{Output change (db)} = 20 \log_{10} \frac{\text{a.v.c. bias}}{\text{a.v.c. bias for } E_{rms} = 2\ \text{V}}$$

$$= 20 \log_{10} \frac{\text{a.v.c. bias}}{-2.2}$$

From this we have for 3.3 db change in signal input voltage (2 db change in diode input) a corresponding output change of 2.4 db. The complete a.v.c. characteristic is tabulated below and plotted in Fig. 27.41.

Change in diode input (db)	A.V.C. Bias Voltage	Change in Signal Input (db)	Change in diode output (db)
0	— 2.2	0	0
2	— 2.9	3.3	2.4
4	— 3.5	6.5	4.0
6	— 4.5	10.6	6.2
8	— 6	16.8	8.7
10	— 7.5	22	10.6
12	— 9.1	27.2	12.3
14	—11.8	33.9	14.6
16	—15	40	16.7
18	—18.5	46	18.5
20	—23.9	52.8	20.7
22	—29.5	60	22.5
22.8	—32	65.8	23.2

It is seen that a change of 60 db in signal input gives an increase of 22.5 db in output. It should also be observed that in most cases it can be taken that the diode input is directly proportional to diode output, and the additional set of calculations need not be made—e.g. 60 db change in signal input gives 22 db change in diode input or 22.5 db change in diode output. For three similar controlled stages the output change would be reduced to 7.5 db. If the valves to be controlled are not of the same type, then individual input-output curves must be drawn and the results combined to give the complete a.v.c. characteristic.

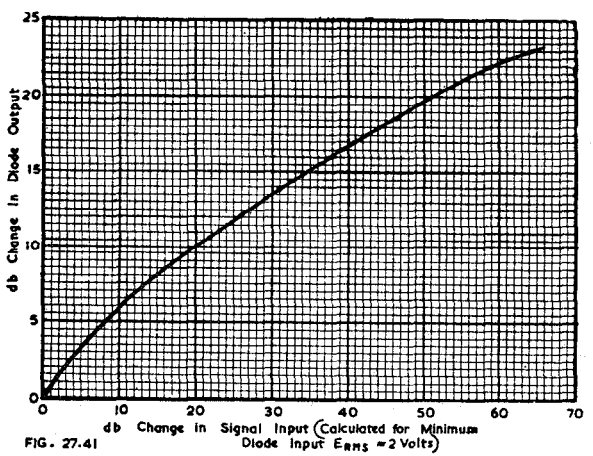


Fig. 27.41. Calculated a.v.c. characteristic for a single controlled stage using type 6SK7.

The a.v.c. characteristic for diode input voltages smaller than $E_{rms} = 2$ volts can be readily plotted, but as the useful range of signal input voltages, where control is mainly required, is usually greater than this value in a reasonably sensitive receiver (and because of the limitations of the diode curves) this value has been taken as affording a satisfactory example.

The variation in gain given by simple a.v.c. is limited, and for very strong signals a local-distance switch or some other method to prevent overloading of the receiver is required.

(3) The voltage amplifier and diode detector used for the previous example are to be used in a delayed a.v.c. circuit, in which the delay bias applied to the diode is -10 volts.

If they are not available, the diode characteristics relating r.m.s. input voltage to d.c. output voltage, for various delay bias voltages, can be measured directly. The rectified voltage, used for a.v.c. bias, is not completely independent of modulation when a delay bias is used, and there is an increase in the available d.c. when the percentage modulation is increased. Usually the a.v.c. comes into operation for lower carrier input voltages than would normally be expected, particularly when the percentage of modulation approaches 100%.

The complete design procedure now follows that given previously for simple a.v.c. using the data derived by the method given in the last paragraph. It should be clear that curve (1) in Fig. 27.40 remains unchanged, but curve (2) must be replotted. The resultant data are then available for plotting the a.v.c. characteristic. For signal input voltages of which the peak value does not exceed the diode delay bias, the receiver operation is the same as for one which does not incorporate a.v.c. (this is clearly shown in Fig. 27.36).

The slope of the no control line is readily determined since it is taken that the output is directly proportional to the input.

SECTION 4 : MUTING (Q.A.V.C.)

(i) General operation (ii) Typical circuits (iii) Circuits used with F-M receivers

(i) General operation

When a sensitive receiver which incorporates automatic volume control is being tuned from one signal to another there is an objectionable increase in noise output. This effect can be overcome by using a circuit arrangement which will make the receiver silent in the absence of a signal. Arrangements of this nature are known by various names such as muting, interstation-noise suppression, quiet automatic volume control (Q.A.V.C.), or squelch systems.

It is desirable, with these circuits, for the receiver to come into operation with the weakest possible useful signal voltage. Since the useful signal voltage may be variable for different conditions of reception, communications receivers are usually fitted with a variable threshold control which can be adjusted to give the best results. For broadcast receivers variable external controls are not used, the muting range being pre-set by the manufacturer.

Most systems of muting depend for their operation on the application of a large bias voltage to an i-f amplifier valve, the detector or an a-f amplifier valve. A wide variety of circuits has been used by receiver designers, but attention will be confined here to a few typical arrangements, since the general principles are much the same in all cases.

(ii) Typical circuits

(a) Biased diode detector

A simple type of biased detector muting system is shown in Fig. 27.42. It is seen that the circuit arrangement for the detector is quite conventional except that the diode load is returned to a tap on the cathode resistor. This makes the diode plate negative with respect to cathode, by the voltage developed between the cathode and the tapping point on the bias resistor R_k and so detection cannot occur until the peak signal input voltage exceeds this negative bias voltage. The components are marked to correspond to those in Sect. 1 of this Chapter.

It should be apparent that there will be a range of signal input voltages around the threshold point over which the audio distortion will be severe.

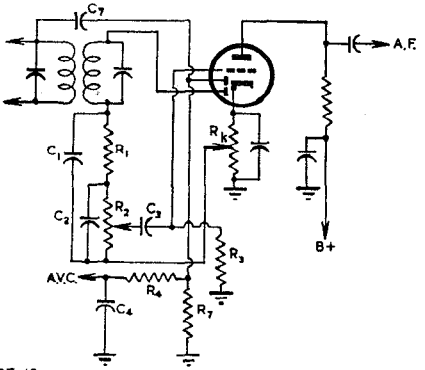


FIG. 27.42 Biased Detector Muting System

A more elaborate muting system, giving improved results over the simple system of Fig. 27.42 has been described by K. R. Sturley (Ref. 44). This uses a negatively biased diode and at the same time the circuit is arranged to provide d.c. amplified delayed a.v.c. The operation of this circuit can be readily understood from Fig. 27.43. The diode marked D_3 acts as the automatic volume control detector, and the d.c. voltage developed across the load resistor R_2 is applied to the grid of the triode section of V_3 and amplified. The diode D_4 will only come into operation when the cathode of V_3 becomes negative with respect to the diode plate, and the a.v.c. bias is delayed until this condition occurs. Considering now the double diode V_2, it is seen that D_1 acts as the detection diode, but it can only detect when the signal input voltage exceeds the negative bias voltage developed across the cathode circuit R_k, C_k. This negative

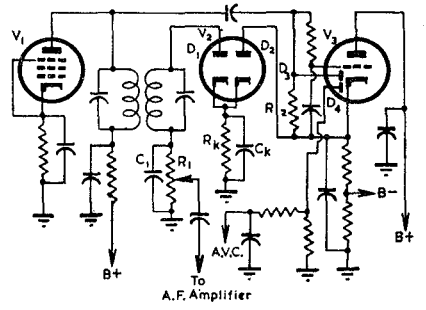


FIG. 27.43 Biased Detector Muting System with D C Amplified & Delayed A.V.C.

bias voltage only exists when the diode D_2 is conducting, which occurs when the cathode of V_3 is positive. As soon as the cathode of V_3 becomes negative, the a.v.c. comes into operation, the diode D_2 no longer conducts, and the negative bias is removed from the plate of the detection diode D_1 which then begins to function in the usual manner. Part of the detected voltage output will appear across R_k, C_k but this is not serious if the value of R_k is very much less than the resistance of R_1 (say about one tenth or less). It is recommended that C_kR_k be made equal to C_1R_1.

(b) Inoperative audio amplifier

A typical arrangement of this type (Ref. 57) is shown in Fig. 27.44. V_1 is any double diode, such as type 6H6, and V_2 is a pentagrid mixer, such as the type 6L7, in which

grid 1 has a remote cut-off and grid 3 a sharp cut-off characteristic. Some systems use two valves in place of V_2 to effect muting and audio frequency amplification. Improved systems are also available (Ref. 54) which use a duo-diode pentode to eliminate the separate double diode valve, the pentode section being used as the intermediate frequency voltage amplifier. Audio a.v.c. is readily applied in this latter case.

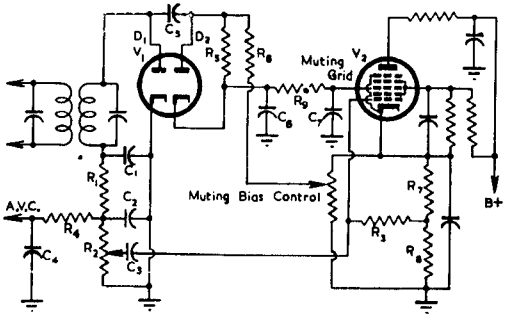


FIG. 27.44 Inoperative Audio Amplifier Muting System

From Fig. 27.44 it is readily seen that the diode detector and simple a.v.c. arrangements are quite conventional. The audio output from the detector is applied to grid 1 of the valve V_2. Only part of the cathode bias is applied to grid 1 by using a tap on the cathode resistor. In the absence of conduction through the diode D_2 there is a large negative bias applied to grid 3 due to the total cathode bias voltage developed across R_7 and R_8 in series. The d.c. path to grid 3 is via R_6, R_5 and R_9. R_6 has a high value of resistance to prevent the plate of D_2 from being connected to ground through the comparatively low impedance of the cathode circuit of V_2 (which includes the muting control as shown). The circuit made up from R_9, C_6 and C_7 is merely a filter to allow the application of direct bias voltage only to the muting grid (3) of V_2; however, R_9 also performs the useful function of stabilizing the voltage applied to grid 3 in the event of the anti-muting bias being sufficiently large to cause grid current. R_5 is the diode load resistor for D_2, and C_5 allows the application of i-f voltage to the plate of the diode D_2. When a signal is received the voltage developed across R_5 is sufficiently large, and of the correct polarity, to reduce the total negative bias on grid 3 and so allow the valve V_2 to perform the function of voltage amplifier for a-f voltages applied to grid 1.

An interesting arrangement (Ref. 54) is shown in Fig. 27.45, in which a duplex-diode pentode and its associated circuit combine the functions of muting, detection, conventional and audio a.v.c., and audio frequency amplification. The valve V_1 is a duo-diode pentode in which grid 1 has a remote cut-off characteristic (the circuit was developed around the Australian-made type 6G8-G). The operation of this circuit is somewhat different from those previously discussed. The maximum gain obtainable from a resistance-capacitance coupled audio frequency amplifier occurs when the negative grid bias has a particular value. For a negative bias less than the optimum value (and for a particular screen voltage, which is generally made fairly low), g_m will drop and the stage will effectively be muted. When the negative bias is made larger than the optimum value the gain of the stage will decrease at a comparatively slow rate. This principle is used in the circuit of Fig. 27.45 and the signal, muting, and audio a.v.c. voltages are all applied simultaneously to the control grid. The cathode resistors R_{10} and R_{11} are used to set the bias voltage to give the optimum value for maximum gain. R_{11} is then adjusted to a lower value to reduce the total bias voltage, and to cause the gain to drop to such a low value that muting has effectively occurred. It is necessary to select the values of bias and screen voltage so that the maximum screen dissipation is not exceeded. When a signal voltage is applied to the a.v.c. diode, the rectified voltage developed across R_7 increases the grid bias

in a negative direction which increases g_m (and so the stage gain) and the valve unmutes. For further increases in signal voltage the a.v.c. comes into operation, and the gain of the audio stage (and also the other controlled stages) begins to fall off in the usual manner. It is seen that only part of the total a.v.c. bias is applied to the grid of V_1.

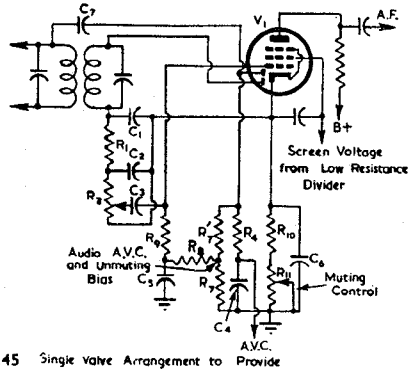


FIG. 27.45 Single Valve Arrangement to Provide Muting, Audio A.V.C., Detection and A.F. Amplification

(iii) Circuits used with F-M receivers

The general principles for muting circuits used in F-M receivers are much the same as for the circuits previously discussed. However, many of the circuits are novel and a few typical arrangements will be discussed.

One typical arrangement (Ref. 59) is shown in Fig. 27.46(A). Valve types V_1, V_2 and V_3 are those normally employed for limiting and detection. Valve V_4 is a double triode with separate cathodes such as the type 6SN7-GT. Section (1) is used as a d.c. amplifier for the muting control bias voltage which is applied to the grid of Section (2). The triode of Section (2) is used as an audio frequency voltage amplifier in the usual manner.

The operation of the circuit is as follows. In the absence of a signal the limiter valve V_2 draws full plate current, and the positive voltage applied to the cathode of triode (1) of V_4 (from the voltage divider R_1, R_2, R_3) is a minimum. At the same time there is a positive voltage on the grid of (1) which is sufficiently large to ensure that there is a resultant positive voltage on the grid with respect to cathode. This allows the plate of (1) to draw full current and makes point A negative with respect to point B across the resistor R_5, and so a negative bias is applied between grid and cathode of triode (2). This bias is made sufficiently large to cut off the plate current of (2) and so prevents any a-f output from being obtained.

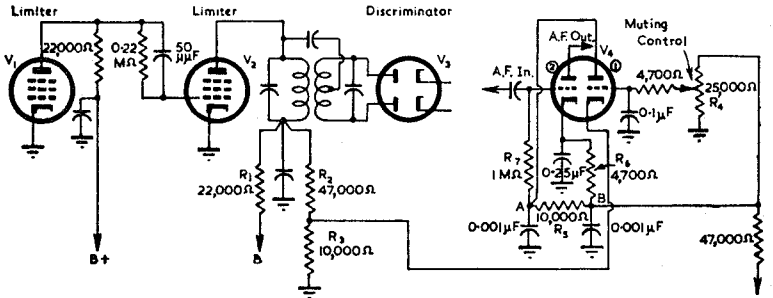


FIG. 27.46(A) Muting System for F-M Receiver

When a signal voltage is impressed on the limiter V_2 the plate current is reduced, and so the positive voltage applied to the cathode of triode (1) (V_4) is increased. When the signal input is sufficiently large the positive cathode voltage will exceed the positive voltage on grid (1) by an amount which is sufficient to cut off the plate current. This puts the points A and B at the same potential and so removes the negative bias from the grid (2). Triode (2) of V_4 then acts as an ordinary a-f voltage amplifier, and its normal bias is obtained from the voltage drop across the cathode resistor R_6.

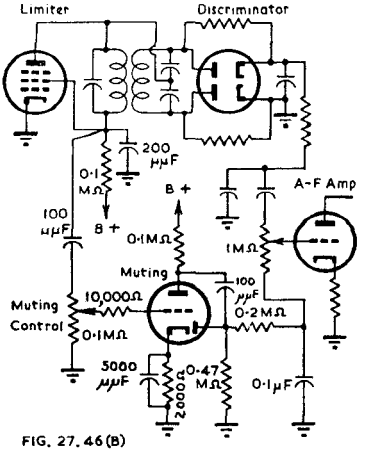


FIG. 27.46(B)

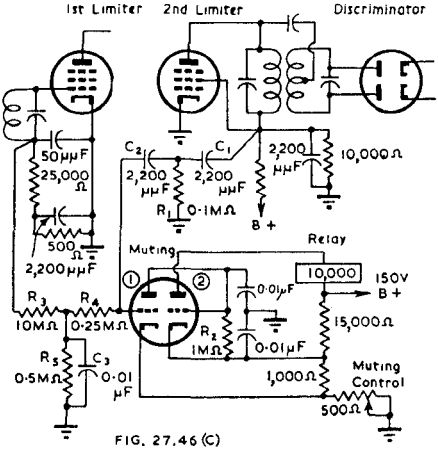


FIG. 27.46(C)

Fig. 27.46(B) shows a simple but effective arrangement for muting. Noise voltages, in the absence of a signal, which appear in the screen circuit of the second limiter valve, are applied to the control grid of the triode section of the muting valve (e.g. type 6AV6) and the amplified noise voltage is applied to the diode detector circuit. The d.c. voltage across the diode load is applied as additional negative bias to the grid of the a-f voltage amplifier valve and cuts off this stage. When a signal is received the noise voltages are reduced and so the additional bias on the a-f valve falls and the stage begins to function in the normal manner.

Another useful arrangement is shown in Fig. 27.46(C). In this circuit noise voltages from the screen circuit of the second limiter are applied to the grid of the muting valve (which could be a type 12AT7) via the high pass filter C_1 C_2 R_1. Triode section (1) operates as an anode bend detector and the direct voltage developed across R_2 cuts off triode section (2) ; the relay is then in the unoperated condition. When a signal is received the noise voltages are reduced due to the receiver quieting, and at the same time additional bias is applied to triode (1) by the rectified voltage appearing at the first limiter grid. The voltage across R_2 is now insufficient to cut off triode (2) and the relay is operated by the plate current. The relay can operate a contact to short the grid of the output valve to earth : additional contacts can also be utilized should the receiver be used for special purposes. The circuit can readily be re-arranged so that the relay is not required, and an additional control bias is made available to cut off the a-f voltage amplifier by increasing the voltage in the cathode circuit in the absence of a signal. The coupling network R_3 R_4 R_5 C_3 has a suitably selected time constant, and the circuit arrangement is such as to prevent amplitude modulation or over deviation of the frequency modulated signal from muting the receiver.

Both of the circuits of Fig. 27.46(B) and (C), or variations of them, have been widely used in f-m mobile and V.H.F. link receivers. In some cases additional negative bias is applied to both the a-f voltage amplifier valve and the a-f output valve ; this has the advantage in the case of mobile receivers that the battery drain is reduced very appreciably during stand-by periods since a large proportion of the battery drain is due to the H.T. current drawn by the output valve.

If muting ON-OFF is required it is usual to switch an additional resistor into the cathode circuit of the muting valve. This resistor is made sufficiently large to cut off the valve and so render the muting inoperative.

A number of other useful circuit arrangements can be obtained from Refs. 58 and 59. Many circuits have appeared in the patent literature, but have not been generally published. One of particular interest uses the two limiters (which are resistance-capacitance coupled) as a multivibrator unit, the output of the second valve being coupled back to the input of the first by means of resistance and capacitance connected in series. In the presence of signal input voltages the relatively low amplification between the valves prevents the feedback network from being effective. In the absence of a signal the grid biases are such that noise voltages will be amplified sufficiently until the circuit operates as a multivibrator. One of the two valves is then always in a non-conducting condition and there is no audio output. This system is described by J. A. Worcester in G.E. Patent Docket 68743. Another useful circuit is given by R. A. Peterson in R.C.A. Patent Docket 21,998. This incorporates d.c. amplification and also requires the use of an additional double diode with separate cathodes. The diodes rectify noise output (which contains A-M) from the limiter. The d.c. voltage developed across the diode load is amplified and applied as a muting bias on the a-f amplifier valve. Unmuting occurs in the presence of a signal by using a negative voltage from the limiter grid to oppose the rectified voltage appearing across the diode load.

Muting circuits are generally applied only to F-M receivers using the limiter and discriminator combination. The noise level between stations with receivers using ratio detectors or locked oscillator arrangements is generally fairly low, and muting is not usually considered to be so necessary in these cases. However, it is a relatively simple matter to utilize the rectified d.c. voltage available at the output of a ratio detector (or also in a conventional discriminator, see Ref. 62 p. 120) to operate a muting system, since the rectified d.c. voltage is proportional to the strength of the incoming signal.

SECTION 5 : NOISE LIMITING

(i) General (ii) Typical circuit arrangements.

(i) General

The purpose of a noise (or crash) limiter in a radio receiver is to assist in the reduction of noise pulses, such as those due to ignition interference and crashes of static, so that their effects may be minimized at the receiver output. The difference between muting systems and noise limiters should be carefully distinguished, as they perform quite different functions in connection with the type of noise which they are meant to eliminate.

Noise limiters in general follow two trends. One group " punches a hole " in the signal so that the receiver output is momentarily cut off. The other main group functions by limiting the maximum output to a value which is not appreciably greater than some pre-determined level.

It can be shown fairly readily (Ref. 63) that the best results for noise reduction can be obtained by placing the limiter in the receiver at a point of low selectivity. The Lamb silencer (Ref. 65) for example, is usually placed after the first i-f stage and its operation is such as to cut off the plate current in the second i-f amplifier valve, momentarily.

For many purposes elaborate noise limiting circuits (Refs. 65, 71) are not essential, and the tendency in the usual communications receiver is to use simple diode limiting to remove noise peaks. For amateur work sufficiently good results are often possible using audio output limiters (see Refs. 66, 67, 68). With the A-M receivers used in mobile communications systems a very elaborate noise limiter may be incorporated.

See also Chapter 16 Sect. 6 for speech clippers and Sect. 7 for noise peak and output limiters.

The threshold of operation for noise limiters can be arranged for either automatic or manual setting for different signal input voltages. Good results are possible using automatic setting, but the more elaborate circuits practically always make some provision for manual control.

(ii) Typical circuit arrangements

The Lamb silencer can be made to give excellent results, but because it is rather elaborate it is not extensively used in commercial communications receivers. For a description of its operation, together with complete circuit data, the reader should consult Ref. 65.

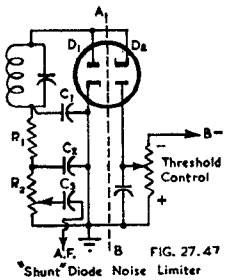


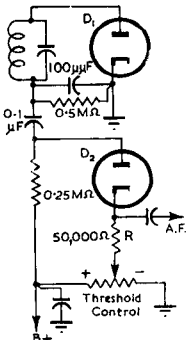
FIG. 27.47 "Shunt" Diode Noise Limiter

Fig. 27.47 shows a typical example of the " shunt " type of diode limiter. It is seen that the circuit to the left of the dotted line AB is the usual diode detector circuit and the component values are identical with those normally selected. The negative direct bias voltage is set to prevent the diode D_2 from conducting until the peak input voltage exceeds the bias. When this occurs the diode D_2 acts as a virtual short circuit, and there is practically no output from the detector circuit.

A " series " type of diode limiter is shown in Fig. 27.48. The diode D_1 is used for detection in the usual manner Diode D_2 is biased to be conducting with normal signal voltages applied to the detector circuit. For bursts of noise there is an instantaneous negative voltage applied to the plate of D_2, and when this negative voltage exceeds the positive bias the diode stops conducting and so opens the audio output circuit. A large amount of audio gain is required when this type of circuit is used, because of the low audio voltage available.

These simple circuits have several disadvantages. Firstly they are both susceptible to hum because of heater-cathode leakage when the cathode of D_2 is above earth. For example this limits the size of the resistor R which can be used in the circuit of Fig. 27.48, and so results in a loss in audio output. (An increase on the value shown would be permissible however). A further disadvantage is that stray capacitances will allow some of the high frequency noise components to appear in the receiver output, even though the diodes are operating in the prescribed manner ; this can be largely overcome with care in layout and wiring to minimize stray capacitances.

Automatic threshold control may be arranged with simple " series " and " shunt " limiters. Suitable methods are given in the references (particularly Refs. 62A, 64 and



"Series" Diode Noise Limiter
FIG. 27.48

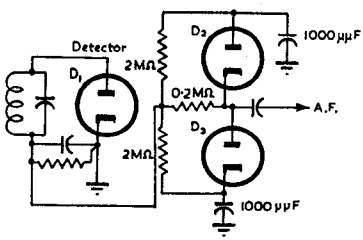


FIG. 27.49 Automatic Noise Limiting Circuit

70). However, a much more satisfactory circuit (Ref. 44) is shown in Fig. 27.49. The diode D_1 is incorporated in the usual detector arrangement and this circuit provides a variable bias voltage for the noise limiting diodes D_2 and D_3. A short burst of noise voltage having a positive polarity will cause the diode D_3 to conduct and so flatten out the audio waveform. A noise voltage having negative polarity causes D_2 to conduct which then flattens out the negative peak of the audio output. In the absence of noise the positive and negative half cycles are equally damped and so distortion is reduced.

Additional methods used for noise limiting in radio receivers are given in Chapter 16 Sect. 7 ; methods of noise reduction for use with reproduction from records are described in Chapter 17 Sect. 7.

SECTION 6 : TUNING INDICATORS

(i) Miscellaneous (ii) Electron ray tuning indicators (iii) Null point indicator using Electron Ray tube (iv) Indicators for F-M receivers.

(i) Miscellaneous

A tuning indicator is a device which indicates, usually by means of a maximum or minimum deflection, when a receiver is correctly tuned. These indicators have taken a number of forms, particularly before the advent of the Electron Ray tuning indicator, originally called the " Magic Eye," and a few of these will be briefly discussed before considering the Electron Ray Tube in detail.

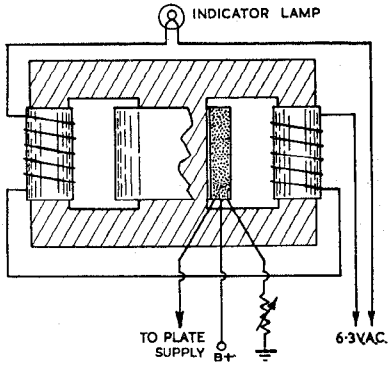


FIG. 27.50 Saturated Reactor Tuning Indicator

One arrangement is to use a milliammeter connected in the plate circuit of a voltage amplifier valve which is controlled by a.v.c. Circuits of this type can also be arranged to indicate relative signal strength, and the meter scale may be calibrated in arbitrary " S " units. Another form is the saturated reactor or dimming lamp indicator. This uses a pilot lamp, in series with a special form of iron-cored inductance, which is excited from a suitable winding on the power transformer. A second winding on the inductance (or transformer) carries the plate current of one or more valves which are controlled by a.v.c. In this simple form the maximum plate current is sufficient to saturate the core and so reduce the impedance in series with the pilot lamp, which is then at full brilliance. When a signal is being tuned the plate current is reduced and the lamp dims. In order to make the pilot lamp reach full brilliance when the receiver is tuned to a station instead of dimming, a " bucking " current can be passed through another winding so that saturation occurs when the plate current is very small, instead of it occurring when the plate current is large. Both arrangements can be understood by studying Fig. 27.50.

A further arrangement is to use a neon tube in which the length of the illuminated column is proportional to the d.c. voltage obtained from a resistance connected in series with the plate of an amplifier valve controlled by a.v.c.

(ii) Electron Ray tuning indicators

Electron Ray tuning indicators are the most popular of all the arrangements being considered. These indicators operate from either the signal diode or the a.v.c. diode circuit. The Electron Ray tube is not limited to use in receivers with a.v.c., since it operates to indicate a change of voltage across any part of the circuit. For example it may be connected to the signal diode circuit irrespective of the presence of a.v.c., or it may be connected across the cathode bias resistor of an anode bend detector. The correct type of Electron Ray tube to be selected for any position depends on the controlling voltage available.

The most popular types of Electron Ray tube (e.g. 6U5/6G5) have a triode amplifier incorporated in the same envelope, so that the voltage necessary to obtain full control is decreased. In most types this amplifier has a remote cut-off characteristic so that the sensitivity may be high for weak signals and yet not cause " overlapping " on strong signals. Type 6E5 has a linear characteristic and is occasionally used for special applications. Type 6AF6-G has two independent Ray-Control Electrodes, one of which may be used for strong signals and the other for weak signals, but has no amplifier incorporated in the same envelope.

In a typical receiver with delayed a.v.c. the Electron Ray tube may be connected to either the signal or the a.v.c. circuit, but since it will give no indication until the diode starts to conduct, it will not operate on weak signals when connected to a delayed a.v.c. circuit. Consequently most receivers using delayed a.v.c. employ the signal diode circuit for operating the tuning indicator. The disadvantage of this latter arrangement is that it introduces additional a.c. shunting effects on the detector diode load resistance and so leads to increased distortion at high modulation levels (see Sect. 1(i) above). The a.c. shunting effects are minimized by using a high resistance in the grid circuit of the tuning indicator, a value of about four times the diode load resistance being typical. In order to prevent flicker due to modulation, adequate decoupling between the diode load and the indicator grid is necessary. A capacitance of about 0.05 μF is usually connected from grid to ground, and this, in conjunction with the grid resistor previously mentioned, should lead to satisfactory operation (see Fig. 27.51). If simple a.v.c. is used (i.e. no delay voltage) it is preferable to operate the tuning indicator from the a.v.c. line to reduce a.c. shunting (see again Fig. 27.51). From the diagram it can be seen that with the switch in the " Det." position the grid of the tuning indicator is connected through a 2 megohm resistor to the detector diode circuit. With the switch in the " a.v.c. " position the indicator is connected directly to the a.v.c. line. This shows the two alternative connections just discussed. The cathode of the tuning indicator is returned to a suitable tapping point on the cathode bias resistor of the power valve as discussed below.

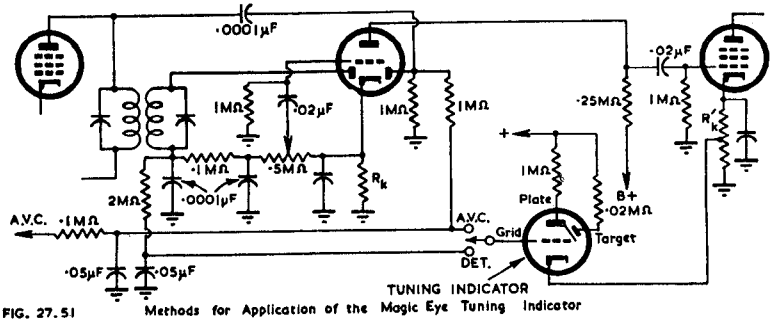


FIG. 27.51 Methods for Application of the Magic Eye Tuning Indicator

The cathode of the Electron Ray tube should be, as closely as possible, at the same potential as the cathode of the diode. If its cathode is more negative than that of the diode, grid current may occur thereby increasing the initial bias on the controlled stages and reducing the sensitivity of the receiver. Consequently if the diode cathode is earthed, the indicator tube cathode should also be earthed, but if the diode cathode is positive then the indicator tube cathode should also be positive by an approximately equal amount. One satisfactory method of obtaining this positive voltage, which however may only be used with a Class A power valve, is to connect the cathode of the Magic Eye to a tapping on the cathode bias resistor of the power valve. With this arrangement it is advisable for the tapping to be adjusted to make the cathode of the Electron Ray tube about 0.5 volt less positive than that of the diode in order to allow for contact potential in the indicator tube, the " delay " due to this small voltage being negligible.

Alternatively, the cathode return of the Magic Eye may be taken to a suitable tapping point on a voltage divider across the " B " supply. Due to the fairly heavy and variable cathode currents drawn by the older types of indicator valves it is essential that the voltage obtained from any voltage divider, or other source of voltage, should not be affected appreciably by a current drain of from 0 to 8 mA. It is for this reason that it is not satisfactory to tie the cathode of the indicator tube to that of the diode. With the newer " space charge grid " construction the cathode currents remain more nearly constant throughout life, and this allowance for change of current need not be made. However, it is not advisable to base calculations for cathode bias resistors on the published values of cathode currents since in some cases with valves of the newer construction, these are higher than the average currents.

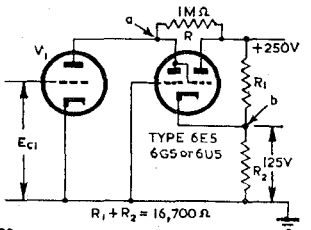


FIG. 27.52 Circuit for Wide-Angle Tuning

Overlapping of the two images is possible on very strong signals, whatever type of indicator tube is selected, but it is generally found with a remote cut-off type (such as the 6U5/6G5) that this is not often experienced under field conditions. Certain arrangements have been devised to reduce the tendency to overlapping, but none is free from criticism. Desensitization of the tuning indicator is readily applied, but affects indications on weak signals. The use of two separate tuning indicators, or a single type 6AF6-G with two separate amplifiers, one for weak and one for strong signals, is excellent but expensive. If the grid of the indicator tube is excited from the moving contact of the volume control the deflection will depend upon the setting of the control, and " silent tuning " will not be possible.

Wide Angle Tuning with a maximum angle of 180° is practicable if an external triode amplifier is added (see Ref. 73). With this circuit (Fig. 27.52) the edges of the pattern are sharp from 0° to about 150° to 180°.

(iii) Null point indicator using Electron Ray tube

A Magic Eye tuning indicator may be used in many applications as an indicating device, one of these being as a null point indicator for use with a.c. bridge circuits. Such an arrangement is preferable to the use of head phones or sensitive instruments, since it may be used without disturbance from external noises and is capable of withstanding considerable overload without damage. The sensitivity of the type 6E5 is 0.1 volt (r.m.s.) for a very clearly marked indication. When used as a null point indicator the 6E5 grid is biased approximately 4 volts negative, and the a.c. voltage is

applied between grid and a cathode. Any suitable pre-amplifying stage may be used to increase the sensitivity of the device if desired. When an a.c. voltage is applied the sharp image will change to a blurred half-tone and as the null point is reached the image will again become sharp. A heavy overload may cause overlapping of the pattern, but this is not detrimental to the tube.

(iv) Indicators for F-M receivers

The usual types of electron ray tuning indicator such as the 6U5/6G5 and 6E5, have been adapted for use as tuning aids in F-M receivers, and several systems using these tubes will be described A special electron ray indicator designed for use in F-M receivers has been described by F. M. Bailey (Ref. 76), and has been commercially released as type 6AL7-GT. Data on the application of the type 6AL7-GT can be found in Ref. 77 and in the R.C.A. HB-3 Tube Handbook.

A method that immediately suggests itself for connecting a tuning indicator to a F-M receiver using a limiter is shown in Fig. 27.53. This method of obtaining a control voltage, from the limiter grid circuit, for operating the indicator tube is by no means the best arrangement available. The disadvantage of the circuit is that, when a strong signal is being tuned-in, the maximum voltage at the limiter grid is not sharply defined, and exact tuning is almost impossible under this condition. The resistor R and capacitor C are used to provide decoupling, as the presence of a.c. components of voltage at the indicator grid will prevent the fluorescent pattern from being sharply defined.

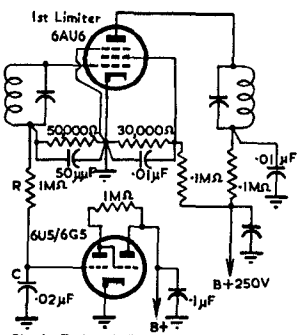


FIG. 27.53 Simple Tuning Indicator Arrangement for F-M Receiver

A much more satisfactory tuning arrangement is shown in Fig. 27.54. This is similar to the Philco Circuit shown in Ref. 75 but the two components R and C have been added. The additional resistor appears to be necessary if the d.c. voltages applied to the diode plates of the balanced rectifier are to be equal when the receiver is detuned by an equal amount above and below the centre frequency. Actual adjustment of R could be made to achieve more exact symmetry, but it is probable that in most cases the tuning operation would not be seriously impaired by leaving R and C out altogether. The operation of the circuit is straight forward. Assume firstly that the receiver is tuned to the centre frequency. The balanced rectifier has no voltage output, and the negative voltage developed across the resistor in the limiter grid is applied to the control grid of the tuning indicator, this voltage causing the pattern to close. When the receiver is detuned there is a voltage developed across R_L, of the polarity shown, due to the operation of the balanced rectifier. This voltage plus that developed in the limiter grid are added algebraically and the resultant voltage is applied between grid and cathode of the tuning indicator. Since the net bias voltage will always be less than that obtained when the limiter voltage alone is applied (the correct tuning position) the pattern on the tuning indicator opens. The indications given by this circuit are sharply defined, and in addition the indicator opens and closes in the same manner as for indicator circuits used in conventional A-M receivers

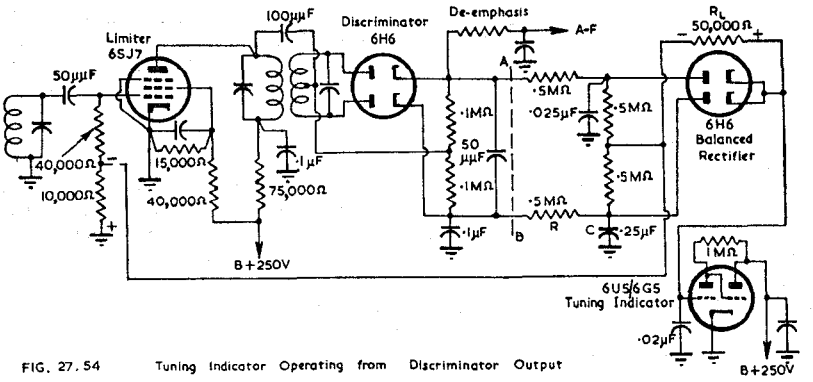


FIG. 27.54 Tuning Indicator Operating from Discriminator Output

This latter feature is not available with similar arrangements operating from the discriminator output alone.

Tuning aids are sometimes used in receivers with ratio detectors. The simplest arrangement in this case is to take the control bias voltage from the a.v.c. take-off point, or to use whatever fraction of this total voltage that is thought to be necessary for operating the tuning indicator.

SECTION 7 : CRYSTAL DETECTORS

(i) Old type crystal detectors (ii) Fixed germanium crystal detectors (iii) Fixed silicon crystal detectors (iv) Theory of crystal rectification (v) Transistors.

(i) Old type crystal detectors

Crystal detectors of the " catswhisker " type have been used for many years, but are very touchy, require frequent adjustment, and are affected by even slight vibration. However, when correctly adjusted, they make quite efficient detectors. Crystal sets are briefly mentioned in Chapter 34 Sect. 1(ii).

(ii) Fixed germanium crystal detectors

These have the advantages of small size and of needing no heater supply, thereby avoiding the possibility of introducing hum into high impedance circuits. Their main disadvantages are that the impedance presented to negative voltages is comparatively low and dependent upon the applied voltage, and that the characteristics from unit to unit show comparatively large variations.

Reverse resistance in a typical case varies from 2 megohms with 20 volts applied to 0.2 megohm at about 100 volts. In some circuits, e.g. a F-M ratio detector, this reverse conductance affects the operation and modifications are required to obtain satisfactory performance. The forward resistance is very low e.g. 200 ohms with one volt applied, falling below 100 ohms at somewhat higher voltages for a typical unit—and this feature can be valuable in some applications.

In this type of rectifier (see Ref. 79 from which this description is taken) as distinct from silicon rectifiers, the outstanding advantage lies in an ability to handle large voltages in the reverse direction, while in the forward direction, the slope (measured at +1 volt) may be of the order of 100 ohms (10 mA at 1 volt).

The slope in the reverse direction reaches a maximum resistance value at the order of −2 volts, beyond which the resistance falls slowly until, at a particular voltage known as the " turnover voltage," the slope resistance falls to zero and then becomes negative.

Measurements of rectification efficiency at various frequencies up to 100 Mc/s indicate that the efficiency falls with frequency by an amount which depends upon the " turnover voltage," the higher the " turnover voltage " the lower the rectification efficiency. In view of this, crystals intended for use at very high frequencies have a maximum as well as a mimimum " turnover voltage " rating.

A typical current/voltage characteristic is shown in Fig. 27.55.

Rectification occurs at the junction between a metallic point and the surface of crystalline germanium. During manufacture this junction is treated to obtain optimum impedance characteristic and time stability. After assembly, the metal point is cemented to the germanium to prevent dislodgment by vibration, and the complete assembly is sealed to prevent ingress of moisture.

A characteristic of fixed germanium crystal detectors is their remarkable property of withstanding severe mechanical shock or vibration. The estimated life of the rectifier is indefinite—in excess of 10 000 hours.

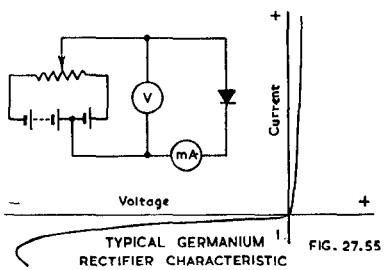


FIG. 27.55

There is little change in rectifier characteristics from 15°C to 50°C, but above this temperature up to 100°C, both forward and back slope resistances decrease slowly.

The characteristics of germanium crystal diodes vary considerably, depending on the application and the manufacturer, but the following data are representative of the majority of types.

Allowable direct current	20 to 60 mA.
Allowable surge current	100 to 600 mA.
Allowable reverse voltage	25 to 250 volts
Turnover voltage (reverse voltage for zero dynamic resistance)	40 to 275 volts
Minimum current with +1 volt	2.5 to 15 mA (some are less than 2.5 mA).
Reverse current with −50 volts applied (this only applies to types having an allowable reverse voltage of 50 volts)	40 to 1660 μA
Capacitance	0.8 to 3.0 $\mu\mu$F.
Maximum ambient temperature	+70° to +85°C.
Minimum ambient temperature	−40° to −55°C.
Maximum frequency	up to several hundred Mc/s.

References to germanium detectors : 78, 79, 80, 81, 83, 84, 85, 85A, 85B.

(iii) Fixed silicon crystal detectors

The fixed silicon crystal detector is principally used as a frequency converter at frequencies above 100 Mc/s. Some designs go up to 1000 Mc/s, while others go as high as 5000 or 10 000 Mc/s. The silicon detector is liable to damage by transient voltage overloads in the reverse direction. The conversion loss is about 6 to 8 db.

References to silicon detectors : 82, 83.

(iv) Theory of crystal rectification

The modern theory of crystal rectification is given in Ref. 83 : See also Ref. 79.

(v) Transistors

Transistors are crystal devices with three or more electrodes, which are capable of amplifying. A good introductory article is Ref. 86. See also Refs. 87, 88, 89, 90, 91, 92, 93, 94, 95, 96.

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